

NOVEL SUBSTRATES FOR IMPROVED COOLING OF POWER ELECTRONICS

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NOVEL SUBSTRATES FOR IMPROVED COOLING OF POWER ELECTRONICS

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NOMENCLATURE

A	Exponent to Arrhenius Equation
a	Crack length
A_{cond}	Area of Conduction
A_h	Nanoindentation tip contact area
A_r	Residual indentation area resulting from Nanoindentation
A_{wick}	Cross Sectional area of wick
C	Experimental crack growth constant
C_d	Diffusion Constant
C_o	Initial Diffusion Constant
C_p	Specific Heat Capacity
CTE	Coefficient of Thermal Expansion
D	Copper Particle Diameter
E_r	Reduced Young's Modulus
g	Acceleration due to Gravity
H	Wick height
h	Nanoindentation tip height
Ha	Hardness
H_v	Latent Heat of Vaporization
h_c	Thermal Conductance
HTC	Heat Transfer Coefficient
K	Wick Permeability
k	Thermal Conductivity

k_e	Effective thermal conductivity
k_b	bond thermal conductivity
K_{Ic}	Stress intensity factor
L	Bond Thickness
L_i	Lateral interface length of a thermal interface
L_x	Length of Fluid path from x location at wick base to point of evaporation
M	Molar Mass of Evaporating Liquid
m	Fatigue Exponent
\dot{m}	Mass Flow Rate
m''	Mass Flux
N	Number of cycles
N_{fa}	Actual number of cycles to failure
N_{ft}	Number of cycles to failure during accelerated testing
n	Stress Exponent
P_a	Partial Pressure of Liquid in Ambient Air
P_{max}	Maximum Load applied during Nanoindentation measurement
P_v	Pressure of Evaporating Liquid
Q	Heat Load
Q_a	Activation energy for creep
Q_d	Activation energy of diffusion
R	Universal Gas Constant
R''	Thermal Contact Resistance
r_{eff}	Effective Capillary Radius
r_n	Nucleation Radius
R_{th}	Thermal Resistance

T	Temperature
t	Thickness
$t_{1/2}$	Half rise time in flash diffusivity model
t_x	time axis intercept in flash diffusivity model
T_a	Ambient Temperature
T_b	Base Temperature
T_j	Junction Temperature
T_m	Mean junction temperature
T_{max}	Maximum temperature in flash diffusivity model
T_s	Surface Temperature
T_{sat}	Liquid Saturation Temperature
T_v	Temperature of Evaporating Liquid
T_w	Water Temperature
$U(A)$	Uncertainty of variable A
V	Dimensionless temperature rise in flash diffusivity model
\bar{V}	Average Fluid Velocity of path through wick
v_f	Fluid Velocity
$v_{\Delta P}$	Fluid velocity due to ΔP
Y	Stress constant

Greek Symbols

α	Thermal Diffusivity
γ	Evaporation Coefficient
ΔP_c	Available Capillary Pressure
ΔP_g	Gravitational Pressure Drop
ΔP_v	Viscous Pressure Drop

ΔT_c	Critical Surface Superheat
ΔT_j	Junction temperature cycle size
ΔT_R	Temperature change from reference
ΔT_{test}	Temperature cycle during fatigue testing
ΔT_{use}	Normal use temperature cycle
ε	Wick Porosity
ε_T	Thermal Strain
$\dot{\varepsilon}$	Strain Rate
μ_l	Liquid Viscosity
ρ	Density
ρ_l	Liquid Density
σ	Stress
σ_l	Liquid Surface Tension
Φ	Material Concentration
ω	Modified Fourier number in flash diffusivity model

SUMMARY

The thermal management of power electronics is critical to the long term reliability of these devices. In this work, three concepts which allow the placement of advanced cooling solutions close to power electronic die are investigated through the creation of advanced substrate technologies. First, two phase cooling was integrated with direct bonded copper power substrates by sintering copper particles directly onto the back side to allow for evaporative two phase cooling. The work experimentally investigated the impact of the thickness of the copper microporous layer as well as its size relative to the thermal test die on the heat transfer performance. The second methodology developed a novel substrate that replaces the DBC by having a cold plate with integrated AlN dielectric and circuit layer. A low-cost bonding method which created a low thermal resistance composite bonding layer was developed and demonstrated which allows low thermal resistance between the die and the cooling fluid. Finally, a third technique which uses a glass interposer with copper vias to bond the power die was investigated as a third packaging methodology. This strategy was explored through finite element analysis. Overall, this thesis presents several new pathways to improving the thermal management of wide bandgap power electronic and RF devices.

CHAPTER 1. INTRODUCTION

1.1 High Power Electronic Devices

Power electronics devices have become important components in low to high voltage electrical applications, including power grid management, electric vehicles, renewable energy devices (e.g., solar cells), and RF communications [1]. Currently many power electronics devices are silicon based; however, there is a trend to push for wide bandgap (WBG) materials such as gallium nitride (GaN) and silicon carbide (SiC) as they are more efficient, handle higher voltages, and operate at higher temperatures and higher frequencies [2-4]. The advancements in WBG materials for power electronics have pushed devices to become smaller while handling more power. Thus, while they are more efficient, the power losses in the smaller devices results in larger power densities than their silicon counterparts, necessitating more efficient removal of heat to maintain low device operational temperatures. To meet the challenges the thermal management approach must be flexible enough to handle a range of power densities while fitting into small form factors required for a number of device applications.

Due to the high blocking voltages available based on the architecture of GaN and SiC electronics, the main application for these semiconductors fall in the field of electrical power conversion [5]. The most prevalent circuit required for power conversion is the inverter which is used to change between DC and AC voltage. These devices are used in electric vehicles (EVs), renewable energy generation (photovoltaic (PV), and wind power), and uninterruptable power supplies (UPS) to convert the source input to the required output [6, 7]. For renewable energy generation in photovoltaic (PV) systems, power electronics

are necessary to convert the DC power and control voltage output to make it grid compatible or for battery charging in home storage systems. It can be used to significantly improve system efficiency by isolating damaged or shaded cells within the PV circuit. Although these devices are typically 96-99% efficient, their reliability is currently below that of the PV cells, making them the weak link in the system [8]. On the grid level power electronics can be applied to integrate several generation systems, (solar, wind, nuclear, oil, etc.) to provide consistent power more efficiently [9]. Implementing a “Smart Grid” control system also makes distributed generation and storage of electricity a feasible option to further improve grid reliability and efficiency. Due to the higher frequency and smaller form factor available to WBG devices, they can also be used for RF signal amplifiers, motor controllers, and PV converters. However, due to the novelty of WBG materials, they have only recently entered the commercial market for high power devices [10].

1.1.1 Power Electronic Device Background

The insulated gate bipolar transistor (IGBT) is a high voltage switch and is an integral component in many different modern appliances, from electric cars and trains, to air conditioners and stereos [11]. As a transistor it is very useful due to the low gate voltage required to drive the high voltage circuit. The IGBT is a normally-off device built on a silicon substrate where the P^+ layer acts as the collector and the N^+ layer as the emitter was shown in Figure 1. When a positive voltage is applied to the gate holes are created in the p-type doped Si, and move to the n-type doped Si. This allows electrons to flow through the p-type Si and to the collector to turn the switch on.

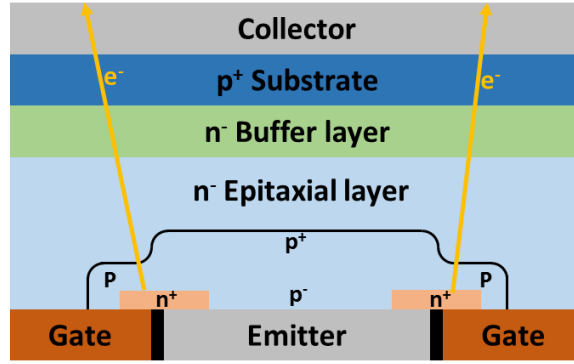


Figure 1. IGBT unit cell showing the location of the collector, emitter, gates, and the semiconductor dopant types used in each area of the device. The direction of electron flow is also shown by the yellow arrows.

Although IGBTs can handle very high voltages (kV range), they can become thermally unstable at high frequencies, and suffer from latch-up which will not allow the device to turn off, [12, 13]. One of the most catastrophic problems is thermal runaway where an increase in the junction temperature leads to an increase in the leakage current in the off-state [14]. When the temperature becomes too high, the device short circuits and the IGBT will burn out, possibly causing damage to the system and other nearby components. Since IGBTs are often used in high power applications where output is greater than about 5 kW, and temperatures are over 100°C significant cooling challenges are present to dissipate the heat, [15]. The chips are also only about 1 to 2 cm², leading to extremely high heat fluxes which must be spread from the device. The silicon substrate, which has a thermal conductivity of ~130 W/m-K, and a maximum temperature of ~125°C, is one of these challenges as it limits heat spreading near the device. Therefore, reducing the thermal resistance later in the thermal stack and improving reliability of the substrate is vital for long term operation.

Another power electronic device often used is the high electron mobility transistor (HEMT) based on WBG semiconductors such as GaN. These devices have become useful devices for applications that require operating at high voltage, power, and frequency. This is because GaN has a high electric field breakdown, good electron mobility, good thermal conductivity, and is stable at high operating temperatures [16]. The values for thermal conductivity of GaN have been reported to be around 150 W/m-K, [17-19] to as high as 253 W/m-K [20] at room temperature. The high thermal conductivity aids in dissipating heat away from the junction. A simplified AlGaIn/GaN HEMT structure is shown below in Figure 2.

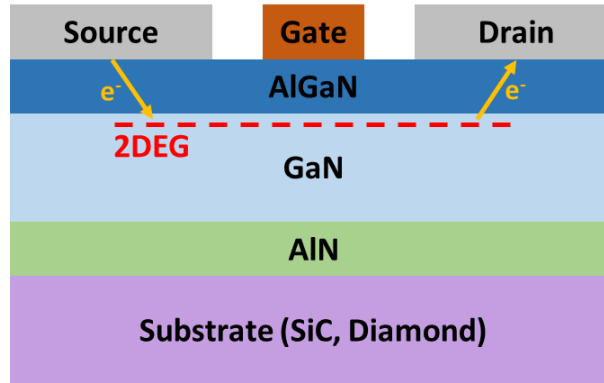


Figure 2. Simplified structure of AlGaIn/GaN HEMT device showing the location of the collector, emitter, gates, and the semiconductors used in each area of the device. The direction of electron flow is also shown by the yellow arrows.

The HEMT operates by using high mobility electrons generated by piezoelectric polarization creating a 2D electron gas (2DEG) which has a current carrier density significantly larger than traditional semiconductors [21]. This is a normally-on transistor, but when a negative voltage is applied to the gate electrons move out of the 2DEG restricting current flow, and turning the device off. Since these devices can operate at higher power densities, there are significant cooling and reliability issues. Although

HEMTs are more efficient than IGBTs, they are also only $\sim 4 \text{ mm}^2$ in size, leading to significantly higher heat fluxes which must be dissipated [22]. Although the thermal conductivity of SiC, (387 W/m-K [23]) is much higher than Si these devices often operate at high temperatures ($\sim 250^\circ\text{C}$) which will degrade the substrate and the materials used to bond the device to it. To ensure reliable operation it is important to reduce the thermal resistance between the substrates these devices are built on and the cooling solution.

1.1.2 Power Device Thermal Stack

The thermal path to reject heat from power electronics devices to the environment is primarily dictated by the electrical, and thermal needs of the device. Due to the high voltage of power electronics devices, the substrate on which the circuit is built requires a large blocking voltage between the power and ground poles. Therefore, the circuits are commonly built on a direct-bond-copper (DBC) substrate, which consists of a ceramic core with a thin copper metallization layer, ($\sim 0.3 \text{ mm}$) on either side. Because of the large heat fluxes ($>100 \text{ W/cm}^2$) it is often necessary to bond the DBC substrate to a metallic heat spreader with the use of solder. This device package is then attached to a heat sink with a layer of thermal grease as shown in Figure 3 below.

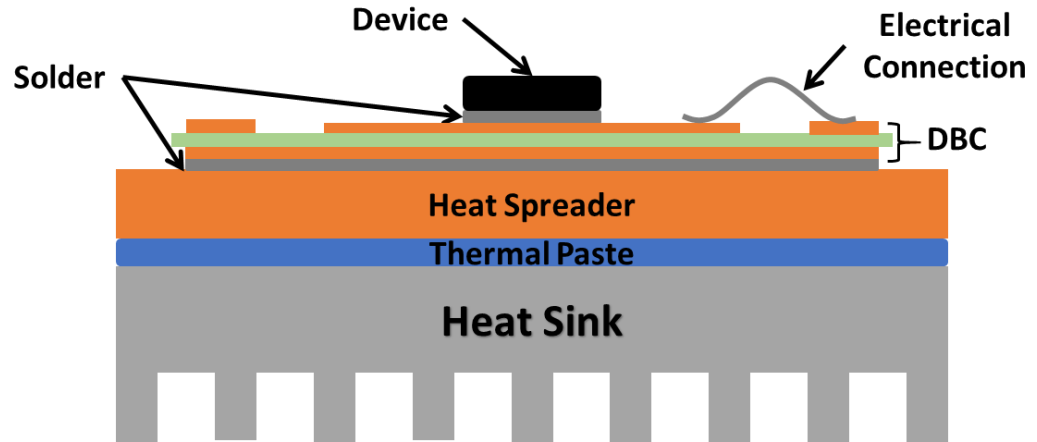


Figure 3. Typical power module package.

In order to provide sufficient electrical shielding, ceramics such as aluminum nitride (AlN), alumina (Al₂O₃), and beryllium oxide, (BeO) are used as a dielectric material due to their high dielectric strength (>10 kV/mm) [24]. Although the thermal conductivity of BeO (260 W/m-K) is larger than AlN (157 W/m-K) and alumina (20 W/m-K), BeO is very toxic and expensive to manufacture [25]. Due to the large blocking voltage required, the ceramic layer must be thick so the larger thermal conductivity of AlN to alumina makes it more common in DBC. The device is attached to one side of the DBC, and the heat spreader to the other, typically using Au-Sn solder [26]. The heat spreader typically consists of either solid metals such as copper, and aluminum, or metal matrix composites (MMC's) such as AlSiC, CuW, or CuMo depending on the type of application [27]. These composite materials take advantage of the high thermal conductivity of the metal, (Al or Cu), while also reducing the thermal expansion coefficient with another material, (SiC, W, or Mo). The heat spreader is then attached mechanically to the heat sink with thermal paste in between [28]. In this thermal path the largest problems usually occur at the layer interfaces due to low thermal conductivity bond material and the possibility of bond

delamination. Removing or replacing these materials can lead to large improvements in thermal management and reliability of the device.

1.1.3 Device Reliability Issues

Power electronics devices play an important role in many industries from power conversion, and renewable energy harvesting to hybrid electric vehicles. Component failure can mean losing functionality in large parts of these systems. For renewable energy harvesting, such as solar arrays. This can mean lost energy and revenue for however long the system is down. For systems which are not monitored, like residential systems, problems may only be discovered after several months using metered data, [29]. This makes reliability an important aspect of design, and for IGBTs thermal cycling, and over-temperature induced failures are two of the most common failure modes [30]. Thermal cycling fatigue, and over temperature is a problem for HEMT devices as well, however they also suffer reliability problems from extended high frequency operation [31].

Over-temperature failures are due to operating above the maximum junction temperature for extended periods, while the thermal cycling failure is due to accumulated damage over the life of the device. Over-temperature failure can cause open circuits, short circuits, and loss of gate control, leading to device burnout. Fatigue failure can cause delamination, voiding, and cracking at connection interfaces [32]. The locations where fatigue failures occur are at interfaces where there is a CTE mismatch such as solders, wire bonds, and the AlN/Cu bonds in DBC [33]. This is due to the strain induced at the material interface caused by the difference in thermal expansion of the dissimilar materials explained by equation 1.1:

$$\varepsilon_T = L_i (CTE_1 - CTE_2) \Delta T \quad 1.1$$

where ε_T is the thermal strain, CTE_1 and CTE_2 are the coefficients of thermal expansion of the two materials, ΔT_R is the temperature change and L_i is the lateral interface length. As shown by this equation, the largest strains are present at interfaces with larger CTE mismatches, and larger overall size. The most common of these failure locations is at the solder layer between the DBC and the heat spreader as this interface has the largest CTE mismatch, shown in Table 1, and the largest lateral dimension [34]. Degradation at this interface can cause a significant increase in the thermal resistance, increasing the junction temperature as shown in Figure 4.

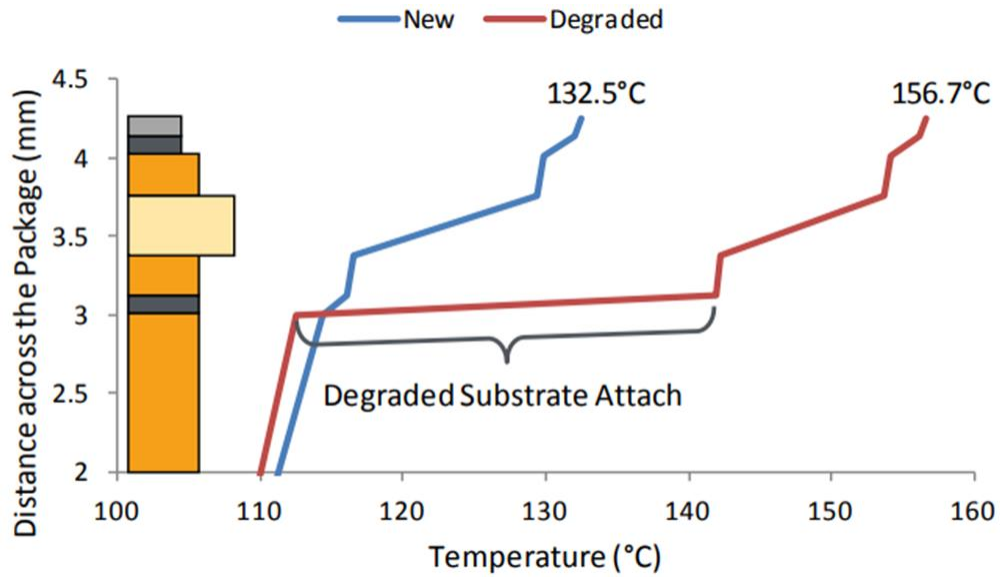


Figure 4. The temperature across the package (from bottom to top: heat spreader, substrate attach, DBC, die attach and device) showing the large increase due to a damaged substrate attach layer [35].

Even partial delamination or voiding at the DBC/baseplate interface will cause an increase in the temperature, and can cause large hot spots depending on the locations of the voids.

If these voids form near the chip location it will cause failure in the chip itself due to over-temperature.

During the normal operation of power electronic devices, they undergo several lower level temperature cycles due to the environment, operating conditions, and on/off cycles. Therefore, it is very important to estimate the life of the bond under thermal loading conditions which cause periodic stresses in the materials. Under cyclic loading conditions crack growth can be described by the Paris' Law [36] shown below by equation 1.2:

$$\frac{da}{dN} = C(\Delta K_{Ic})^m \quad 1.2$$

where a is the crack length, N is the number of cycles C is an experimental constant, ΔK_{Ic} is the change in the stress intensity factor from the maximum and minimum stress states, and m is the fatigue exponent. For most metals m tends to be in the range of 3 – 5 but m is ~2 for aluminum [37]. The stress intensity factor K_{Ic} is determined by the crack geometry, described by crack size a , constant Y , and the stress and is described by equation 1.3.

$$K_{Ic} = Y\sigma\sqrt{2\pi a} \quad 1.3$$

Although other equations exist for different crack shapes, equation 1.3 describes a worst case scenario, therefore it allows for a conservative estimation of crack growth. Due to the power relationship between crack growth and stress, this can have a significant impact on the life of the device. Combining equations 1.1, 1.2, and 1.3 it can be seen that the most effective ways to reduce stress and increase device lifetime is to use two materials with similar CTE values, and to reduce the temperature. As can be seen in Table 1, the CTEs of

Al and Cu are much larger than AlN [38], and Silicon. Metal matrix composites (MMC's) such as Aluminum Silicon Carbide (AlSiC) and Copper Molybdenum/Tungsten (CuMo, CuW) on the other hand have CTE values comparable to Si and AlN, along with comparable thermal conductivity values to Al and Cu. Because of this MMC heat spreaders can significantly improve reliability, and are often used to replace the pure Cu and Al spreaders used in the past.

Table 1. Thermal conductivity and CTE of substrate materials.

Material	Coefficient of thermal expansion (CTE) ($10^{-6}/^{\circ}\text{C}$)	Thermal Conductivity (W/m-K)
Copper	16.5	385
Aluminum	22.2	205
Aluminum Nitride (AlN)	4.5	175
Silicon	4.0	148
Silicon Carbide (SiC)	4.0	120
Aluminum Silicon Carbide (AlSiC)	8.0	185
Copper Molybdenum (CuMo)	7.2	200
Copper Tungsten (CuW)	6.7	175

Decreasing the size of the junction temperature cycle also has a significant impact on the life of the device. As is shown in Figure 5 below, the number of cycles to failure for an IGBT chip is a function of both the mean temperature (T_m), and the temperature cycle of the junction (ΔT_j). By providing more efficient cooling both T_m and ΔT_j can be decreased, and lead to significant improvements in device lifetime.

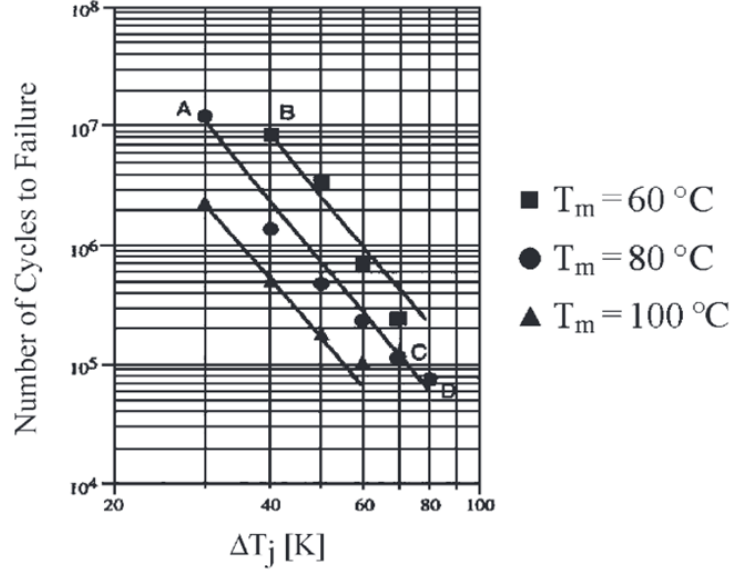


Figure 5. Cycles to failure vs. difference from the junction temperature, for several mean temperatures (T_m), and junction temperature cycle size (ΔT_j), [39].

Temperature reduction can be achieved several ways, one being by decreasing thermal boundary resistance at the interface, or also by decreasing the layer thickness. Using an MMC in the thermal stack after AlN would reduce the bond line stresses by reducing the difference in the CTE while also potentially reducing temperature. Forming a coherent bond between the AlN and MMC could therefore significantly increase the number of cycles to failure of the system.

1.2 Current Bonding Methods

1.2.1 Eutectic Bonding Methods

In the current state of power electronics, there are several main locations within the thermal stack, shown in Figure 3, where it is necessary to bond two dissimilar materials together. First the dielectric material, (AlN, Al₂O₃, or BeO), needs to be bonded to the copper metallization layer so that circuits can be built on it. The metallization is performed

by bonding copper with a Cu/O eutectic melt process shown in Figure 6, below the copper melting temperature [40]. First the copper layer is put in contact with the ceramic layer, and temperature is increased while controlling the flow of O_2 . The oxygen diffuses into the copper and eventually reaches the eutectic composition where a thin layer melts, and after cooling the un-melted copper is left bonded to the ceramic surface. Due to the high processing temperature where the bond solidifies, there are significant residual thermal stresses present after cooling back to room temperature.

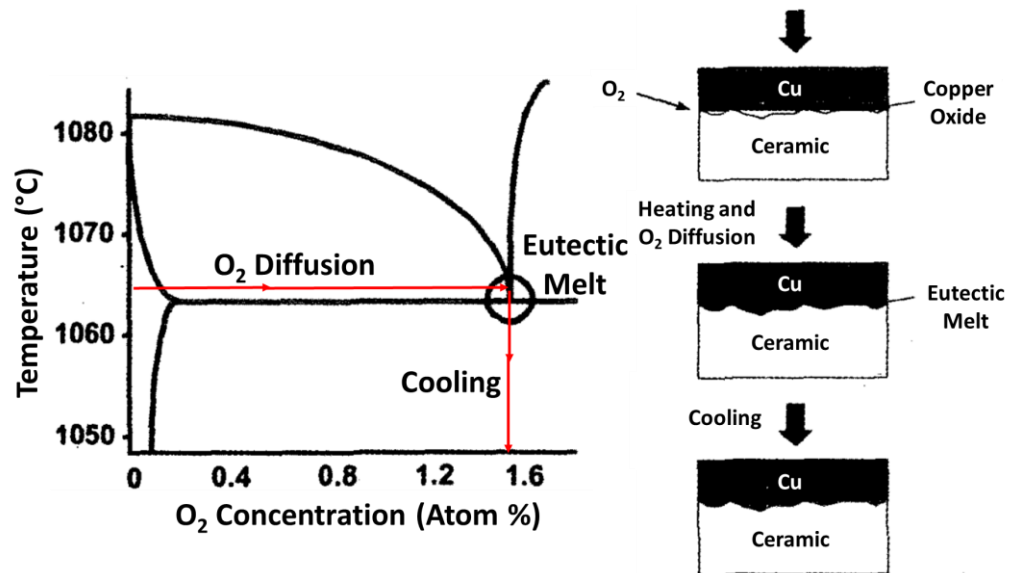


Figure 6. Copper bonding process showing the diffusion of oxygen, eutectic melt temperature of 1065°C, and the cooling and solidification process, [40].

By bonding thin copper foils, with thicker ceramic layers the composite coefficient of thermal expansion becomes only slightly higher than the CTE of the ceramic. Since many power electronic devices are built on silicon or SiC (with a CTE of $4 \times 10^{-6}/^{\circ}C$), this improves the reliability of the die attach bond as explained in section 1.1.3 previously. This same process can also be used to attach two metal layers together to form a strong cohesive bond. This bonding method does however reduce the thermal and electrical conductivity

of the base metal due to the inclusion of foreign atoms in the crystal structure. These atoms cause scattering of the electrons which are the primary heat carrier in metals, however this can be minimized by using a low percentage of the second material. A similar process has also been developed for direct bond aluminum (DBA) where the Al is bonded with an Al/Si eutectic phase [41]. Although this method is extremely effective for making strong bonds, due to the high processing temperatures it cannot be used to attach the device to the substrate. However this method could potentially replace solder to attach the DBC to heat spreader, or heat spreader to heat sink if all components meet the temperature requirements. In this work a similar transient liquid phase eutectic bonding method for attaching the AlN dielectric layer directly to an AlSiC heat spreader was used and will be detailed later in Chapter 3.

1.2.2 Die Attach Methods

In order to mount the device to the DBC, an electrically conductive die attach material with a low processing temperature is required. Typically solders are used for this, although conductive adhesives, and even sintered silver have been used, as summarized in Table 2. These materials can also be used at the DBC/heat spreader interface, or heat spreader/heat sink layer. The type of die attach material used is heavily based on the specific application and must satisfy certain requirements. The material must be able to bond to both the die, and the substrate, thermal conductivity must be sufficient to dissipate heat, and CTE should be similar to both die and substrate [42]. Also, the processing temperature should not exceed the maximum device temperature, and the material should not degrade at the temperature the device will operate at.

Table 2. Thermal properties of selected die attach materials [43].

Material	T _{melt} (°C)	T _{max} (°C)	Thermal Conductivity (W/m-K)	CTE (10 ⁻⁶ /°C)
Au88Ge12	356	320	52	12
Au80Sn20	280	250	58	16
P-1011^a	-	350	1.29	37
H20E-HC^a	-	300	3.5	26
H20E-HC^a	-	200	9.96	53
QMI-3555R^b	400	300	80	16
FO-3, FO-13^c	450	300	60	25
Tape 3M^d	-	250	-	-
Ag nano^e	-	500	240	19

a - Adhesives made by Epoxy Technology.

b - Silver filled glass made by Loctite.

c - Silver filled glass made by ITME, Poland.

d - Thermally conductive tape made by 3M.

e - Ag nanopowder made by AMEPOX Ltd., Poland.

Solders usually offer the best compromise between these requirements, however they are prone to creep and fatigue failure mechanisms [44, 45]. Creep is a thermally activated, time dependent process where a material will plastically deform under constant stress and at elevated temperatures. Due to the CTE mismatch at the interface between the device and substrate, stress is induced in the solder layer at high temperatures. Creep can be described by the Dorn Power Law [46, 47] shown by equation 1.4:

$$\dot{\epsilon} = A\sigma^n \exp\left(-\frac{Q_a}{RT}\right) \quad 1.4$$

where $\dot{\epsilon}$ is the strain rate, A is a material dependent constant, σ is the thermally induced stress, n is the stress exponent, Q_a is the activation energy, R is the universal gas constant and T is the temperature. This will lead to significant increases in the strain rate due to even small temperature changes. After extended periods of time at elevated temperature, the

solder will eventually form voids, and can delaminate, causing significant increases in both electrical and thermal resistance.

In order to mitigate the problems with solder, several bonding methods with silver have been developed, such as sintering silver, and silver filled glass or epoxy [48, 49]. Silver filled epoxy is often used to attach Si dies directly to a metal lead frame due to the large CTE mismatch between Si and Cu. The lower elastic modulus of epoxy allows for less stress transfer between the die and substrate [50]. However metal-filled epoxies are often not suitable for high temperature WBG devices which can operate higher than 250°C [51]. Silver has been sintered as low as 280°C, but has a significantly higher melting point of 961°C, allowing for high temperature operation [52]. Sintered silver has also been shown to have superior electrical, thermal, and mechanical properties compared to solder. The thermal conductivity, electrical resistivity, and elastic modulus are 220 W/m-K, $4\text{e-}6\ \Omega\text{-cm}$, and 10 GPa respectively [53]. The porosity due to the sintering process reduces the elastic moduli below that of pure silver, reducing the stress transferred between the die and the substrate. However due to the cost of silver sintering, solder is still the preferred die attach method, but for new WBG devices with high operating temperatures sintered silver is often the only viable method.

1.2.3 Heat Sink Thermal Interface Materials

To attach the heat spreader to the heat sink and a thermal interface material (TIM) such as thermal grease is typically used to increase the thermal contact area. Due to the irregularities on the surface of the heat sink and heat spreader solid contact between the two surfaces can be on the order of a few percent of the total area [54]. The TIMs are

typically fluid or very malleable in order to fill the gaps left by the solid-solid contact as shown in Figure 7. Types of TIMs include silicone grease with filler particles, epoxies, gels, and low melting alloys [55, 56]. A comparison of the thermal resistivity of several types of TIM materials is shown below in Figure 8.

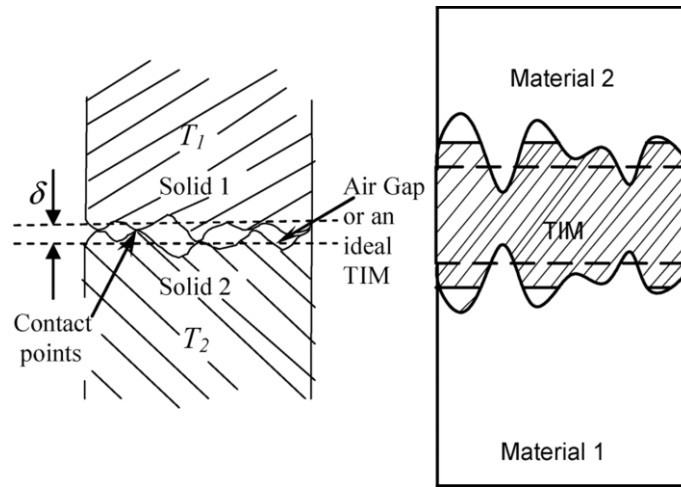


Figure 7. Solid-Solid contact (Left) showing the low contact area available with improved contact area (Right) achieved by adding a TIM material [55].

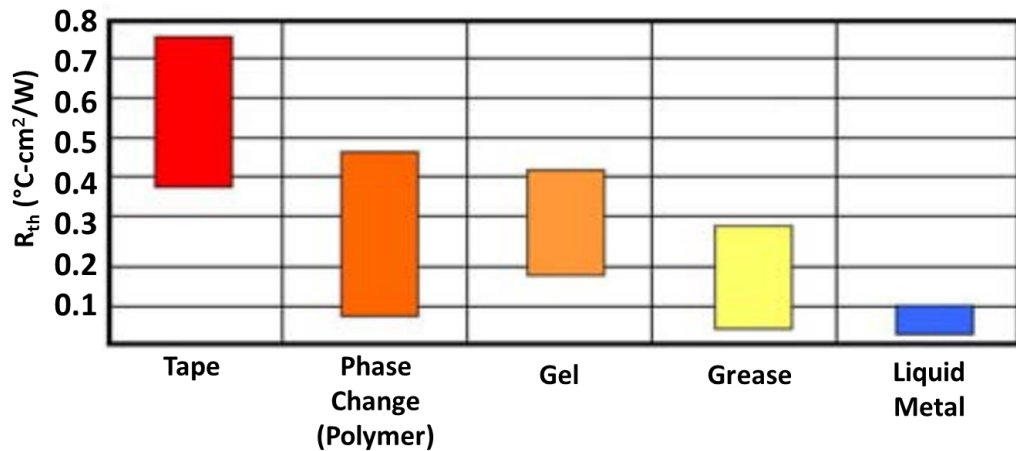


Figure 8. Range of thermal resistivity values showing the relative scale for selected TIM materials [57].

Thermal grease tends to have a higher thermal conductivity ($\sim 1\text{-}10\text{ W/m-K}$ [28]), but since it does not cure thermal cycling can cause grease pump-out and phase separation. Over long periods of time at high temperatures, they can also dry out, reducing the reliability. Epoxies and gels on the other hand are easier to use in manufacturing processes, and the material will not pump out due to being solidified, but they have lower conductivity. Polymeric materials can also form voids after thermal cycling, and do not flow into crevasses as easily. Low melting alloys have the highest thermal conductivity, but are susceptible to dry-out and voids, as well as corrosion at high temperatures [57]. Due to the variation amongst TIMs, the selection is highly dependent on the specific system and manufacturing requirements. In order to solve these problems, this work removes these TIMs all together by integrating evaporative cooling onto the DBC and bonding the dielectric layer directly to the heat sink. This not only decreases the thermal resistance of the stack, but improves reliability by removing a layer that is prone to degradation.

1.3 Cooling Solutions for Power Electronics

Thermal management systems in use today for power electronics include convective air cooled heat sinks, liquid cold plates, integrated micro-channel and fins, jet impingement, and two-phase boiling or evaporation, and are reviewed by Kang *et al.* and Mudawar [58, 59]. The relative heat transfer coefficients achievable are shown in Figure 9 for several heat transfer mechanisms with different types of fluid. Although air cooled systems can be used to dissipate large amounts of power, they also require a large surface area, and do not spread the heat efficiently, making them non-ideal for high power density devices. For cooling at the heated surface where heat fluxes are the excess of 100 W/cm^2 , forced convection and boiling would be the only suitable cooling mechanisms [59].

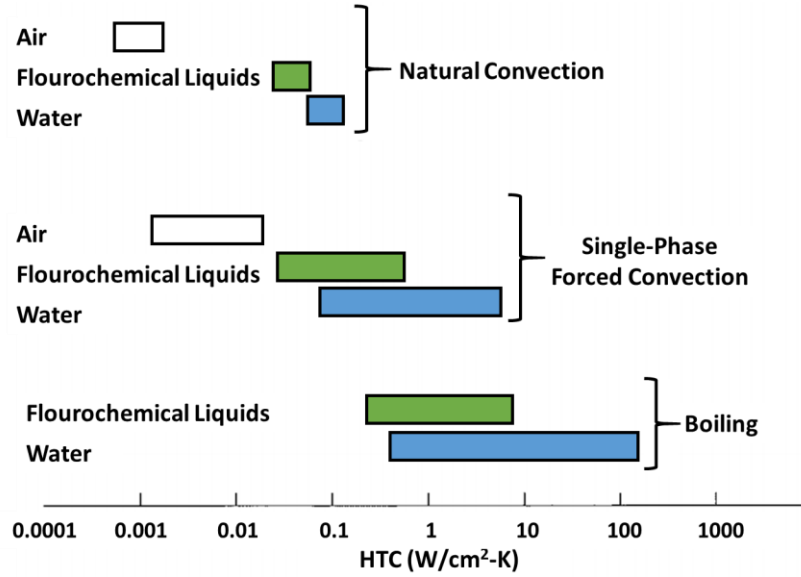


Figure 9. Heat transfer coefficients achievable by natural convection, forced convection, and boiling with several different types of fluids [59].

To more efficiently spread heat to air cooled fins heat pipes and vapor chambers can be integrated into the heat spreader at the source to increase the heat transfer coefficient as high as $0.6 \text{ W/cm}^2\text{-K}$ [60]. This method however introduces two more thermal interfaces where failures may occur as described in sections 1.2.2 and 1.2.3. In order to remove these thermal interfaces many attempts have been made to integrate cooling directly into the heat spreader, and DBC layers, reducing not only thermal resistance, but size and weight [61]. Single phase cooling with micro pin-fins and micro channels integrated into the DBC have been shown to be able to dissipate heat fluxes even in excess of $\sim 1000 \text{ W/cm}^2$ for very small areas (2.45 by 2.45 mm) [62]. These liquid cooling techniques can be used for single side or dual side cooling of IGBT's as has been shown by several researchers to be very effective at increasing power densities. Another versatile implementation of the single phase direct liquid cooling is the Danfoss Shower Power, which employs distributed jets

to shower the surface with fluid [63]. By evenly distributing the jets, the surface temperature can be maintained at a more even temperature.

While these single phase directly integrated cooling methods are efficient cooling schemes, they require external pumping and a heat exchanger to cool the working fluid, adding to overall system complexity. By integrating a thermosiphon or other gravity/capillary fed condenser into the flow loop, the higher heat transfer coefficients of two-phase cooling can be leveraged without the need of external pumping [64]. To further improve performance surface enhancements such a metal foam, have been shown to reduce thermal resistance while increasing the critical heat flux (CHF) [65, 66]. The use of nanoparticles in water has also been shown to increase the boiling CHF by as much as 200% to 1680 kW/m^2 [67]. With nucleate boiling from a microporous surface, the HTC can be increased to well over $\sim 150 \text{ kW/m}^2\text{-K}$, with areas larger than 10 by 10 mm, [68, 69]. Another two-phase option is to use evaporation, which offers heat transfer coefficients of $\sim 15 \text{ kW/m}^2\text{-K}$, larger than forced convection, with water as the working fluid, [70]. The disadvantages are that pool boiling requires a large area for the vapor to expand into, can only occur when the surface temperature is above the boiling point, and does not work in all orientations.

The use of microporous media has been shown to significantly enhance two-phase heat transfer by increasing the effective surface area, and aiding in the delivery of fluid to the heated surface through capillary action. The sintering of copper particles is a well-established manufacturing process to create microporous materials, and has been used to produce capillary wicks for heat pipes with several different sizes of copper particles [71, 72]. These copper wicks are able to deliver fluid to the heated surface without the need for

additional pumping, however these microporous surfaces are limited by the viscous pressure drop which must be overcome [70]. If the wick is unable to deliver sufficient liquid to the heated surface, dry out will occur, increasing the temperature rapidly until device failure. By reducing the copper particle size the available capillary pressure is increased as they are inversely proportional terms. However this increases the viscous pressure loss which is inversely proportional to the square of the particle size, creating a need to balance these two parameters [73, 74]. Work by Weibel *et al.* has elucidated the impact of various particle sizes and microporous layer thicknesses on the evaporation and boiling performance of monodispersed microporous layers applied to copper substrates [75]. However there is little work on irregularly shaped particles and how it may affect the ability of the wick to deliver fluid to the heat source.

Many of these cooling methods add considerable volume and weight to the electronic components, and require heat to be conducted away from the source first, before being rejected by convection. To address this the Defense Advanced Research Projects Agency (DARPA) has started the ICECool (Intra/Interchip Enhanced Cooling) program [76]. This program is working to develop embedded cooling systems which target high heat flux areas of the system with a combination of high thermal conductivity materials and convectively cooled microchannels similar to the concept shown in Figure 10.

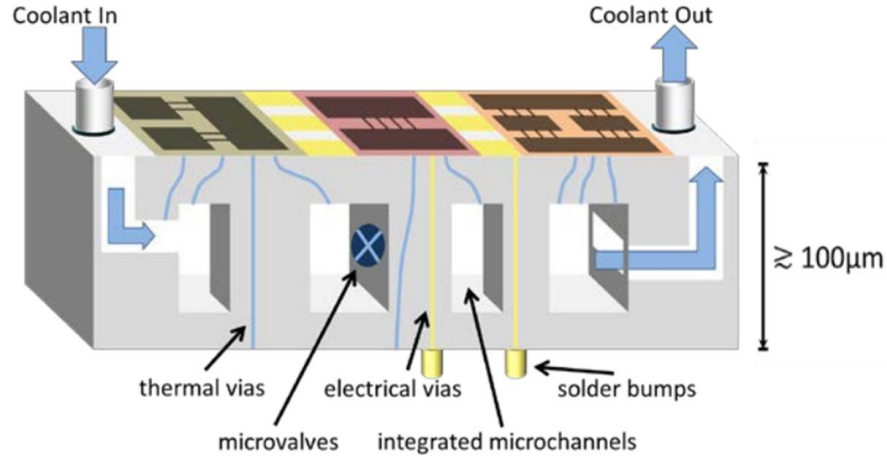


Figure 10. Conceptual ICECool chip [77].

This program has been divided into two individual thrusts, ICECool fundamentals and ICECool applications. The goal of ICECool fundamentals is to demonstrate chip-level heat removal in excess of 1 kW/cm^2 with local micrometer scale hot spots of heat fluxes exceeding 5 kW/cm^2 . The goal of the ICECool applications portion is to integrate these approaches into real systems such as GaN RF amplifiers, and high performance computing modules such as IBMs power 775 supercomputer [78]. Successful approaches have been shown by several studies that combine the high thermal conductivity of diamond with microchannels to increase the power output of GaN RF amplifiers by as much as 3X [79-81]. By embedding these microchannel cooling techniques directly into the chip substrates several thermal resistance layers can be removed to increase the dissipated heat load while reducing the total size/weight of the package.

1.4 Outline of Present Work and Contributions

The work presented here attempts to address the cooling and reliability issues of power electronic devices by reducing the number of layers in the thermal stack to introduce

cooling closer to the power device. This approach improves reliability by removing the layers most prone to failure and degradation, (i.e., solder joints, thermal grease), while also reducing the junction temperature by decreasing the thermal resistance. In order to achieve this, three different methods will be presented which remove different layers of the thermal stack. Finite element modeling will then be used to show the potential improvements which result from using each method in application. Modeling will also be used to show how the systems performance could be changed by adjusting certain experimental parameters.

First, in Chapter 2, a method for integrating evaporative cooling directly onto the backside of a DBC power substrate with sintered copper particles will be presented. In order to evaluate the capillary performance of the wick, three different samples of the same surface area were fabricated with different thicknesses of copper particles. Then another set of three samples were made with the same thickness wick, but three different surface areas to investigate the heat spreading capability. These samples were partially submerged in water and heat was applied to the backside with a platinum heater in order to simulate a device. The device temperature was measured for different applied heat loads and used to compare the cooling performance of each sample. This experimental data were used with several analytical models for capillary fluid flow to estimate how performance would change depending on changes to the particles size, porosity, and other wick parameters. By directly integrating evaporative cooling with sintered copper particles on the back side of the DBC the high thermal resistance solder, and thermal grease layers were removed along with the high CTE heat spreader. Modelling showed that this approach would be able to reduce the device temperature under certain conditions.

In Chapter 3, the thermal stack is reduced through a novel bonding approach which attaches the AlN directly to an AlSiC baseplate. The bonding method and composition will be detailed to explain the transient liquid phase (TLP) bonding technique. The bond line was imaged with scanning electron microscopy (SEM) and energy-dispersive X-ray spectroscopy (EDS) in order to measure the thickness and determine the final chemical composition. The thermal conductivity of the bond was measured with laser flash diffusivity in order to validate its thermal performance. The Young's modulus and hardness were measured with nanoindentation in order to verify its mechanical performance. These physical properties were then used in finite element models to compare the thermal performance of the AlN/AlSiC bond to a standard DBC/solder bond. The thermo-mechanical stresses in the AlN and the bond material were also modeled with finite element modeling and compared to a standard DBC/solder model. By replacing the solder and the bottom Cu layer on the DBC a high thermal conductivity bond the stresses in the materials were reduced while maintaining the same thermal performance.

In the future work section a new type of GaN RF amplifier package is with a glass fan-out and an integrated micro heat spreader was modeled with finite element modeling. The package was modeled with different thicknesses and area of the copper heat spreader. Then the copper heat spreader was replaced with a diamond in order to investigate the potential gains possible by using the high thermal conductivity material. The novel package was then modeled on a CuMo heat carrier, and a large heat spreader with several different heat transfer coefficients applied to the backside of the heat spreader. This way it was determined what type of cooling would be required in order to maintain the package below its maximum operating temperature. The modeling was able to show that integration of a

micro heat spreader into an RF device package allowed for better heat spreading, and significantly reduce the junction temperatures.

The overall objective of this work was to introduce several novel approaches to removing layers of thermal resistance within the power electronics package. The study also aimed to improve the reliability of these devices by reducing the stress within bonds which causes delamination and cracking. By performing this type of large scope study on many different methods, a path for moving forward was revealed which will help to reduce both device temperatures and improve reliability.

CHAPTER 2. EVAPORATIVE COOLING FROM SINTERED COPPER PARTICLE SURFACE

2.1 Introduction

As discussed in Chapter 1, one of the concepts to improve the cooling of power electronic components is to move the liquid cooling solution closer to the device. In this chapter the integration of liquid cooling directly on the backside of the direct bonded copper (DBC) power substrate will be investigated. Integration will be in the form of passive cooling involving evaporation where a sintered porous copper wick is attached to the backside of the DBC. Liquid is transported from a water reservoir from one edge of the wick to the hot spot created on the DBC by a thermal test chip. The goal is to investigate the impact of the wick thickness, size, porosity, and particle size along with device input power on the overall cooling performance which will be shown through several experiments and models. The potential improvements of directly integrating evaporative cooling on DBC will be shown with numerical modeling of a representative IGBT package with integrated cooling.

2.2 Microporous Surface Fabrication

In order to evaluate both the effects of wick thickness and area, six different substrate samples were fabricated of various dimensions. The copper microporous surface was made by sintering irregularly shaped copper particles, (99.5% pure and average size $9.6 \mu\text{m} \pm 1.5 \mu\text{m}$), commercially available from 3M, to a DBC substrate. The DBC substrate was commercially obtained from Curamik, Inc. and consisted of a 0.63 mm aluminum nitride

(AlN) layer with 0.3 mm layers of copper bonded to either side. The DBC samples were cut to size out of a larger DBC plate using an OMAX waterjet, and then cleaned with a 25% HCl solution, DI water, and isopropanol before the sintering process. To manufacture the wick, the copper particles were placed on top of the DBC in a graphite mold, held together by stainless steel plates as shown below in Figure 11.

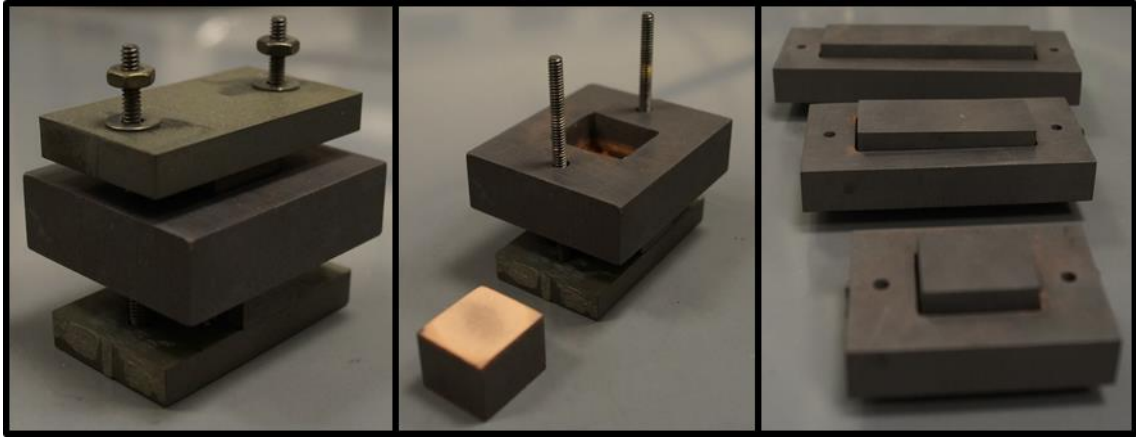


Figure 11. Graphite sintering molds, closed 17 mm by 15 mm (Left), open 17 mm by 15 mm (Center), and closed 20 mm by 25, 50, 75 mm (Right).

The particles were sintered in a tube furnace set to reach 750°C in 55 min, held there for 30 min, and then the power was turned off and the samples cooled back to room temperature naturally. The tube was initially held under vacuum, (~ 20 mTorr), before the furnace was turned on to remove air from the system. For the first 20 min of heating, H_2 gas was flowed at 100 SCCM to reduce any oxides left on the surface, and then Ar gas was flowed for 120 min after that at 500 SCCM for the rest of the heating, and during most of cooling. The copper particles were imaged with an SEM before and after the sintering process as shown below in Figure 12.

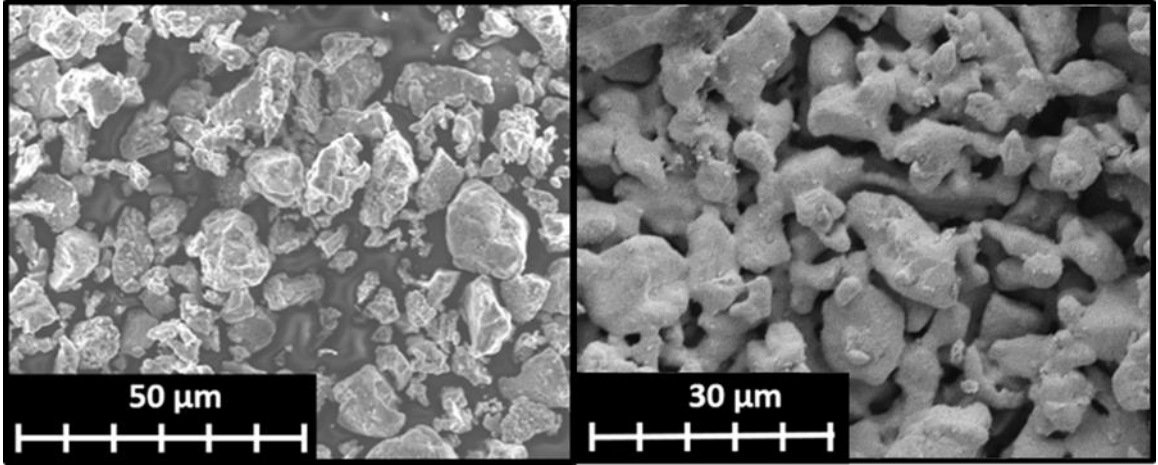


Figure 12. SEM image of $\sim 10\ \mu\text{m}$ 3M particles before, (Left) and after (Right) sintering them to the DBC substrate.

Seven samples in total were fabricated for testing, three were made 15 mm by 17 mm in size, and 3 were made 20 mm high by 25, 50, and 75 mm wide, and one 15 mm by 17 mm samples was made to measure porosity. The 15 mm by 17 mm samples were sintered with varying amounts of copper particles in order to make wicks with different thicknesses. The 20 mm high by 25, 50, and 75 mm wide samples were sintered with an amount of copper particles such that they would all have the same wick thickness, and only the wick width would change. The mass of copper particles, and thickness of DBC alone was measured before sintering, and the total thickness was measured afterward in order to determine the thickness of the wick alone and estimate the porosity. This wick thickness, porosity, and associated standard uncertainty is summarized below in Table 3 for all six samples fabricated. The standard uncertainties were calculated based on a method described by Bell [82]. Table 3 shows that all 7 wicks had similar porosities, within uncertainty, implying that wicking behavior due to capillary affects and vapor escape behavior should be similar. The last wick made was sintered on copper foil and was made much thicker than the other wicks to reduce the relative uncertainty in the Cu mass, and

volume measurements. This allowed the porosity to be measured with a lower uncertainty, and this porosity was applied to the model for all samples since it was made with the same process, and thus should have the same porosity.

Table 3. Summary of sample porosities, wick thicknesses, and associated uncertainties.

Sample Number	1	2	3	4	5	6	7
Sample Size (mm x mm)	17 x 15	17 x 15	17 x 15	20 x 25	20 x 50	20 x 75	17 x 15
Cu Particle Mass (g)	1.058	0.792	0.553	2.006	4.013	6.017	4.077
Wick Thickness (mm)	1.138 ±0.065	0.903 ±0.065	0.636 ±0.065	1.099 ±0.051	0.995 ±0.051	1.118 ±0.025	4.581 ±0.036
Porosity (%)	63.1 ±5.1	61.2 ±5.1	62.9 ±5.1	61.0 ±1.8	58.5 ±2.1	61.5 ±0.9	60.8 ±0.4

2.3 Thermal Test Chip Fabrication

The thermal test chips were attached to the back side of the DBC substrate to apply the thermal load and act as a resistance temperature detector to measure the junction temperature. The thermal test chips (10 mm x 14 mm) were fabricated on a 100 mm silicon wafer that was 300 μm thick. First, the wafer was cleaned in a piranha acid solution, and a 2 μm layer of SiO_2 was grown on top using chemical vapor deposition to provide an electrically insulating layer. Next a serpentine patten of metal was deposited using a photolithography liftoff process as shown in Figure 13 below. A 300 \AA Ti adhesion layer was applied with a sputter coater, and a 0.2 μm layer of platinum was applied on top of that. Third, a 0.5 μm thick Cu layer contact pads were patterned at the end of the platinum lines on which electrical connections were soldered. The copper contacts were made using a Sn-Au-Cu solder (SAC 305) which had a eutectic melting temperature of $\sim 220^\circ\text{C}$ so this was considered the temperature limit of the test chip.

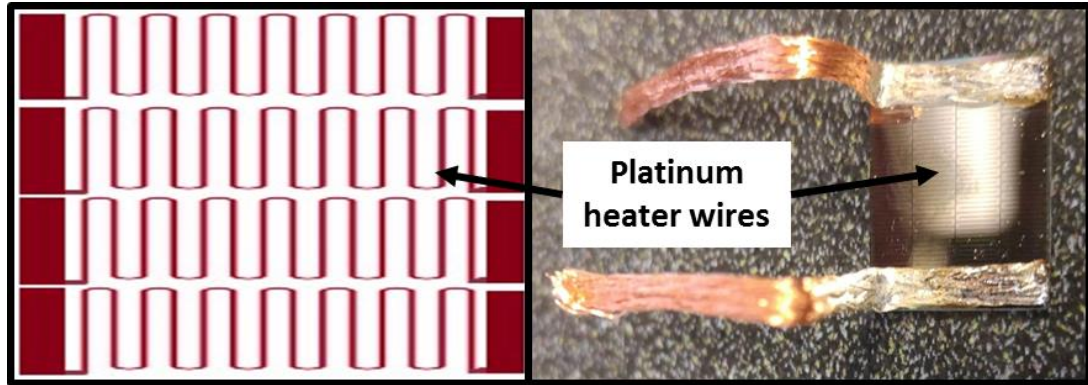


Figure 13. Test Chip heat pattern diagram and final 14 mm by 10 mm test chip with soldered copper leads.

The temperature of the thermal test chips were measured using electrical resistance thermometry. The thermal coefficient of resistance (TCR) for the platinum heaters was calibrated using a thermal stage and Raman spectroscopy. Using the temperature/Raman shift coefficient of a well-known material such as silicon [83] the true surface temperature of the metal heater can be estimated when attempting to extract the metal's TCR. The temperature of the thermal stage was increased from ambient up to 160°C, and the shift of the Raman signal peak of the Si was measured. This created a correction factor between the temperature reading of the thermal stage and the temperature of the Si test chip. By comparing the electrical resistance to the corrected chip temperature, the TCR could be extracted for each test chip as shown in Figure 14 below.

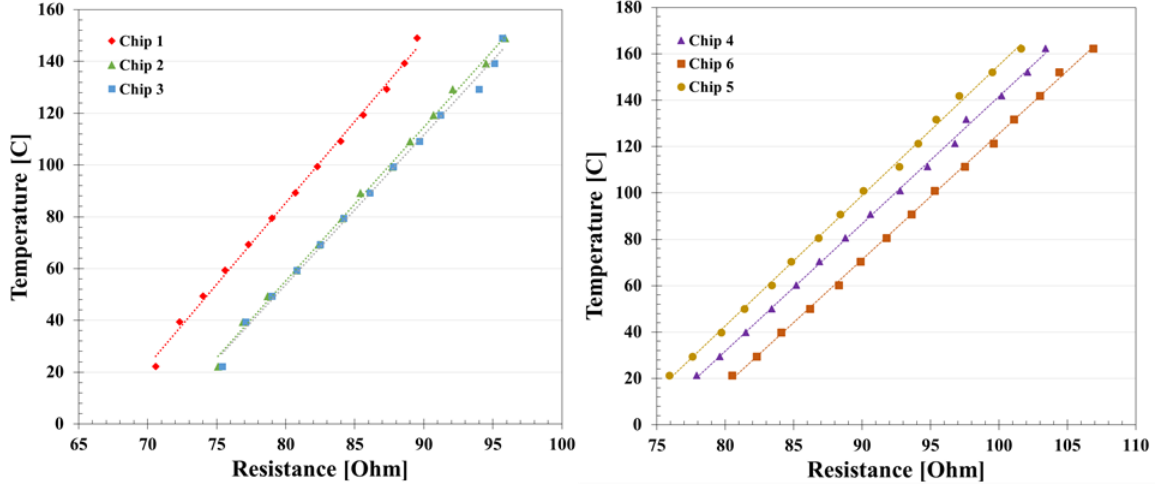


Figure 14. Calibration curves for heaters of the six samples test chips used in the study. The TCR ranged from 0.1588 - 0.1843 $\Omega/^{\circ}\text{C}$.

2.4 Experimental Set Up and Procedure

2.4.1 Experimental Setup.

The thermal test chips were bonded to the sintered DBC substrates using a thermal epoxy called EPO-TEK H2OE with a thermal conductivity of 2.5 W/m-K. Once the chips and substrates were connected, the epoxy was cured on a thermal hot plate set at 85°C for 3 hours. The same bonding procedure was repeated with two pieces of Si wafer with average thicknesses of 305.2 and 305.8 μm respectively. The average total thickness of the two pieces of Si after bonding was found to be 641 μm , giving a bond thickness of 30 $\mu\text{m} \pm 5.2 \mu\text{m}$. Following this, the substrates were inserted into a 3D printed sampled holder made of low-density acrylonitrile butadiene styrene (ABS), thermal conductivity of 0.21 W/m-K, where they were affixed using JB Weld epoxy with a thermal conductivity of 0.59 W/m-K. The low density plastic, and low thermal conductivity bond helped to minimize heat losses due to conduction. The sample holder was then placed in a 3D printed ABS bowl

designed to maintain the water level 2mm above the base of the sample for water uptake as depicted in Figure 15. A peristaltic pump was used to keep the evaporation bowl water at a constant level, by continuously filling the bowl and allowing the water to overflow into a larger collection container where it was then recirculated. This recirculation method also helped to increase the size of the thermal reservoir and kept temperature rise in the water below 10°C over the course of the experiment.

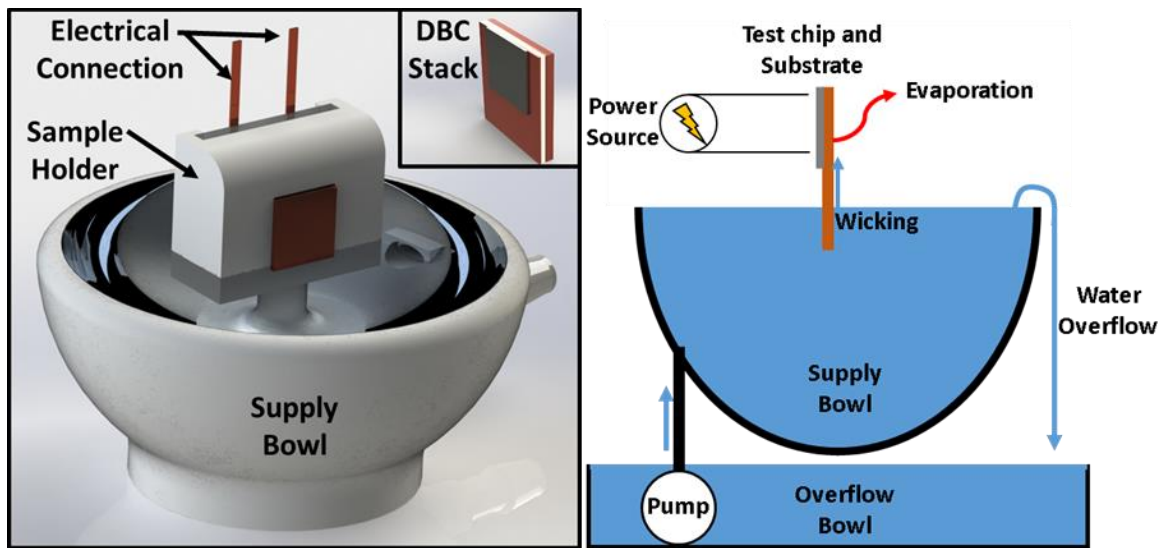


Figure 15. Example ABS plastic sample holder for 17 mm by 15 mm sample showing the electrical connections and the DBC stack, and a simplified diagram showing the partially submerged substrate to wick the water from the supply bowl and the water overflow used to maintain the liquid level.

2.4.2 Error estimations and uncertainty

A finite element analysis was performed in order to verify that there were minimal conductive losses from the DBC sample into the ABS plastic during experimentation. The FEA was performed only on the sampled holder rather than the bowl/sample holder/water system together as shown in Figure 17 below. Convective boundary conditions were applied to the outer surface of the ABS sample holder with a convective heat transfer

coefficient of 10 W/m-K. This value was an estimation based on several natural convection correlations reviewed by Khalifa [84]. To account for the thermal epoxy, and JB weld a thermal conductance of 83,000 W/m²-K was applied between the DBC and chip, and 5900 W/m²-K was applied between the DBC stack and the ABS plastic. The thermal conductance, h_c , was computed from equation 2.1 given below:

$$h_c = \frac{k}{t} \quad 2.1$$

where k was the thermal conductivity of the bond material, and t was the thickness of the bond line being 30 μm for the thermal epoxy, and 100 μm for the JB Weld. The experimentally measured chip temperature was applied as a constant boundary condition to the Si chip surface. The experimentally measured power was then applied to the outer surface of the DBC as a total heat output boundary condition, as displayed in Figure 17 below. In order to ensure solution output was not dependent on the mesh size the mesh was refined until the output heat load changed by less than 2% as shown in Figure 16.

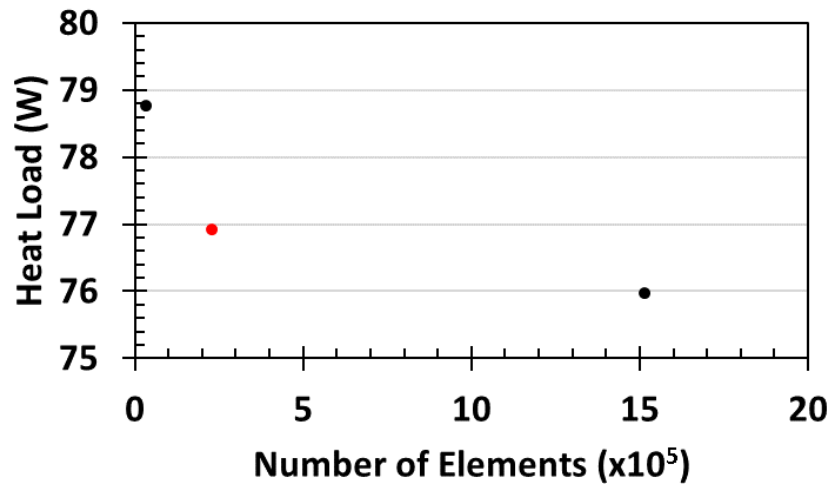


Figure 16. Example solution output as a function of the number of elements in the mesh, showing the mesh size used for further modeling indicated by a red data point.

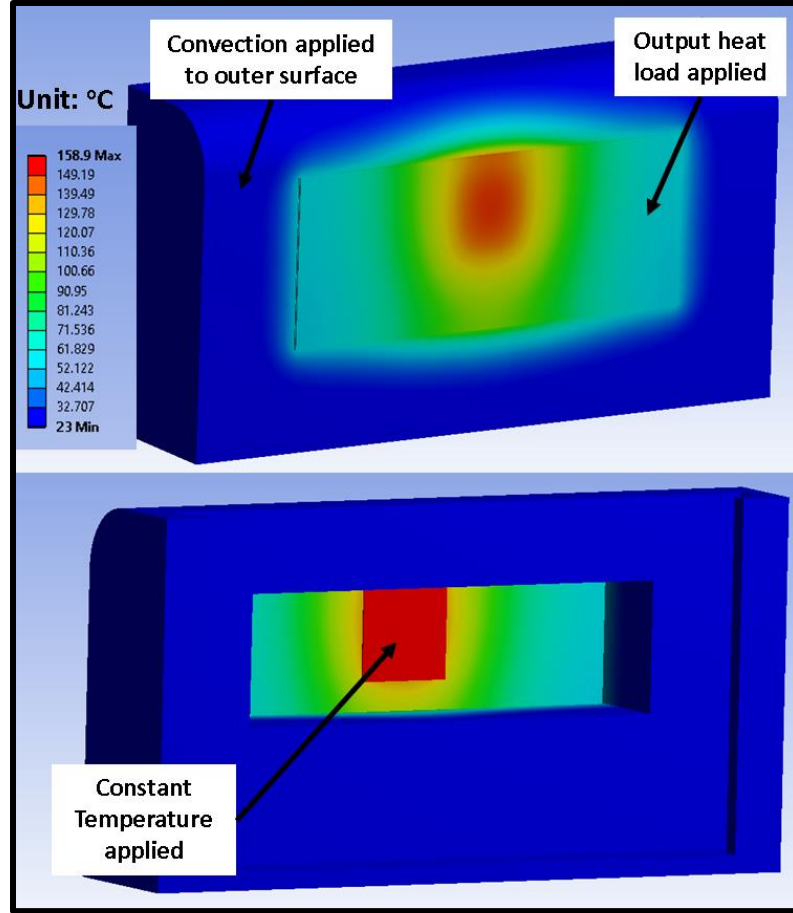


Figure 17. Example of modeled temperature distribution using the 50 mm sample with the location of the applied experimental temperature, (158.9°C), and applied heat load, (99.6 W).

The mesh independence procedure was repeated for all the sample holder sizes, (15, 25, 50, and 75 mm), until the solution output changed by less than 2%. The model was then run and the resultant total heat output from the Si chip was read from the model, and used to compare to the applied heat output to estimate the maximum heat loss due to conduction to the sample holder. The uncertainty was modeled at the conditions of the highest chip temperature for each sample as the largest temperature difference from ambient also leads to the largest heat flow to ambient. The boundary conditions applied to each model, the resulting total power output, and error was summarized below in Table 4. The effect of

losses from radiative heat transfer were also considered, however this was estimated to be less than 0.1 W of total heat dissipated. The percent conductive loss was subtracted from the applied heat load and used in later computations where an applied heat load was used.

Table 4. Summary of conductive heat loss to sample holder.

Sample	15mm	25mm	50mm	75mm
Chip Temperature (°C)	158.2	175.6	158.9	161.6
Evaporative Power Output (W)	74.2	104.5	99.6	104.3
Total Power Output (W)	76.7	109.3	104.8	109.0
Conductive losses (%)	3.31	4.39	4.93	4.38
Number of Elements	230317	442938	566634	687557

The water, and ambient air temperatures were measured with K-type thermocouples with uncertainties of $\pm 2.2^{\circ}\text{C}$. The surface temperature distribution was measured from the FLIR camera using the emissivity of water, 0.98, since the porous Cu surface was wet, and water is opaque to IR. The test chip resistance was measured with a 4-wire configuration by a Keithley 2425 100W source meter, and converted to temperature using the TCR values computed from the calibration curves shown in Figure 14. The uncertainty of the resistance measurement was $\pm 0.2 \Omega$, leading to a total uncertainty of the temperature reading from the test chip to be an average of $\pm 2.2^{\circ}\text{C}$ for sample numbers 1, 4, 5, and 6 while it was $\pm 2.3^{\circ}\text{C}$ for samples 2 and 3.

2.4.3 Experimental Procedure

To run the experiments, the supply pool was filled with DI water and circulated using the peristaltic pump. Power was applied to the heater until either the temperature

limit of the heater was reached, or the maximum power of the power supply was reached. The power was increased from ~ 5 W until one of the limits was reached by increasing the supply current by 0.1 A. Once the voltage reading reached steady-state a picture was taken using the FLIR camera, and the thermocouple readings of the ambient air (T_a), water temperature (T_w), and surface temperature (T_s) were recorded along with the voltage and current measurements as shown in Figure 18.

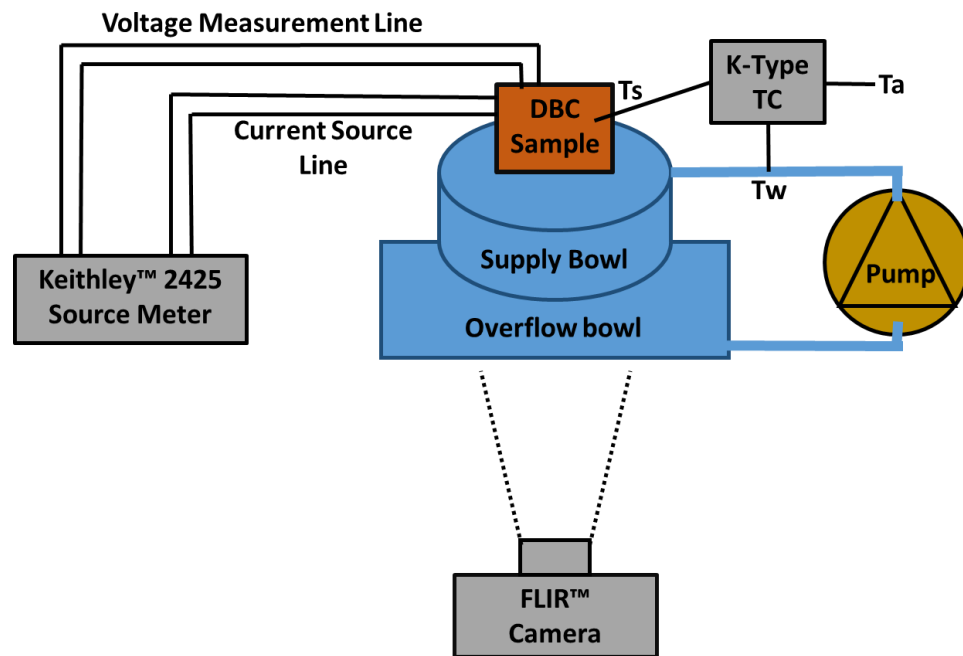


Figure 18. Experimental schematic showing the configuration of the sample being tested. The FLIR camera, the power source and the pump.

The current and voltage measurements were used later to calculate the applied power, and the resistance of the thermal test chip which was then used to compute the chip temperature. The surface temperature, T_s , was measured at the middle of the sample, and ~ 7 mm below the top, which represented the centre of the test chip, and the highest temperature on the surface. On the 17 by 15 mm samples this temperature was measured along with another

surface temperature below the water level at the base. On the 20 by 25, and 50 mm samples two additional surface temperatures were measured at mid-height, and ~5 mm from the edge of the samples. On the 20 by 75 mm sample another two points were measured at mid height between the central point, and the edge points as shown below in Figure 19.



Figure 19. Wick samples mounted in sample holder showing the location of the test chip with a dotted line, and the location of the surface temperature measurements with a crossed circle.

2.5 Results and discussion

2.5.1 *Effect of changing wick thickness*

After the data were collected, the thermal resistance was computed using equation 2.2, where T_j was the chip temperature, T_w was the temperature of the inflow water, and Q was the applied heat load.

$$R_{th} = \frac{T_j - T_w}{Q} \quad 2.2$$

The computed thermal resistances values were plotted against power for the 17 by 15 mm samples in Figure 20 and showed very similar behavior across different wick thicknesses. These thermal resistance values were also similar to values found by Ivanova *et al.* in a study with a DBC integrated heat pipe using a fiber wick [85], although in this study the water temperature was between 40°C and 75°C.

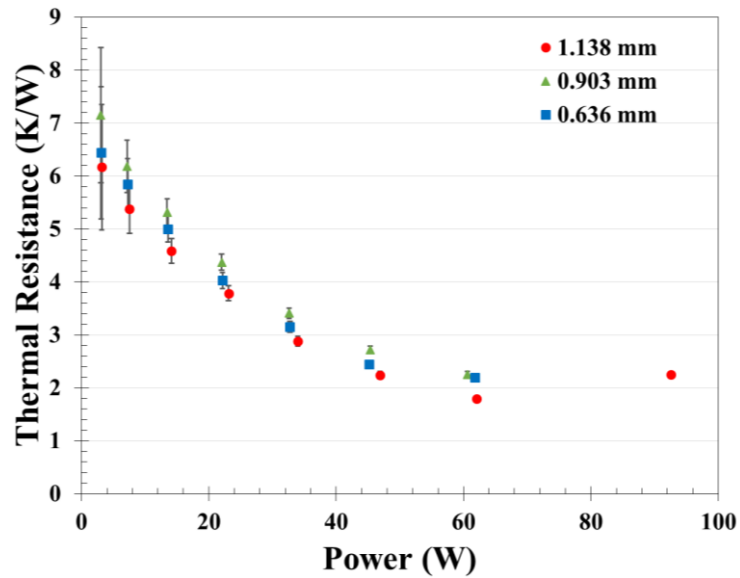


Figure 20. Thermal Resistance of 1.138, 0.903, and 0.603 mm thick samples plotted as a function of heat load, showing the similar behavior across different wicks as heat was increased.

At low power levels the uncertainty was very large due to the fact that $(T_j - T_w)$ was on the same order of magnitude as the uncertainty in that computation, 3.1°C. As the power was increased it can be seen that sample 1, the 1.138 mm wick, had a lower thermal resistance than the other two wicks by a small margin. This wick was also the only one that was able to have the current increased to 0.9 A without burnout. The other two samples

passed the melting temperature of the Pb-Sn solder, ($\sim 180^{\circ}\text{C}$), when the power level was increased and were not able to continue operation. This was partially due to the fact that the thermal test chips used with samples 2 and 3 were manufactured earlier using a Pb-Sn while sample 1 was made using SAC 305 solder with a melting point of $\sim 220^{\circ}\text{C}$. The increase in thermal resistance of the 1.138 mm wick above 80 W was due to the wick reaching dry out where water was no longer able replenish the wick as fast as water was boiling away. This was apparent during experimentation as the surface temperature suddenly increased from $\sim 100^{\circ}\text{C}$ to $\sim 150^{\circ}\text{C}$ as shown in the surface temperature plot in Figure 21. The surface temperature increased until $\sim 100^{\circ}\text{C}$ for each wick, indicating that nucleate boiling had initiated. The temperature then remained constant as power increased, until eventually the wick surface began to dry out, and the temperature increased significantly.

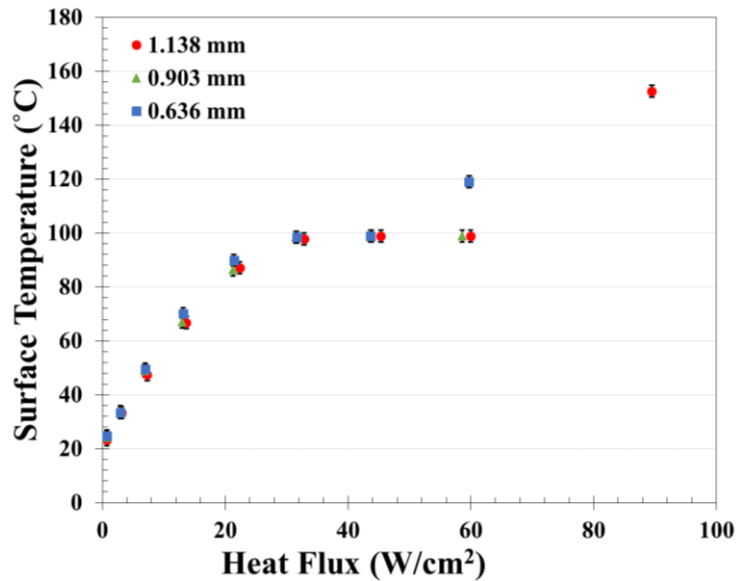


Figure 21. Plot of surface temperature vs. the heat flux for the 1.138, 0.903, and 0.636 mm thick wicks, showing the location where the surface temperature increased above 100°C and the wick began to dry out.

In the surface temperature plot it can clearly be seen for the 1.138 and 0.603 mm samples where the temperature suddenly increases and surface dry out occurs. However the exact heat flux and temperature could not be recorded for the 0.903 mm sample due to sample burn out and solder melting. Using the last resistance measurement and the applied current of 0.9 A, it was estimated that the power was at least 85 W. It was also assumed that the thermal chip failed at 180°C, (the melting point of the Pb-Sn solder), and since the last temperature difference measured between the T_j and T_s was 56°C at 60 W, the surface temperature can be estimated to be at least 124°C. This would place the data point between the 1.138, and 0.603 mm samples. These results were similar to those found by S.-C. Wong that showed a decrease in wick thermal resistance around 40 W, and a significant increase around 80 W for irregular particles with a 0.4 to 1 mm wick thickness, [86]. This result implies that the main cause of dry out for these samples was the ability of the wick to feed water to the boiling area, as increasing the thickness increased the power until dry out. This data also indicates that the resistance to vapor escape was not a significant factor to operational performance as all wicks performed similarly until dry out.

To estimate the temperature at the interface between the DBC, and the copper particles a 1D resistance network was constructed using equation 2.3 to compute the thermal resistance of each layer, and equation 2.4 to compute the total resistance:

$$R_{material} = \frac{t}{k_{material} A_{cond}} \quad 2.3$$

$$R_{th} = R_{Si} + R_{epoxy} + R_{AlN} + 2R_{Cu} \quad 2.4$$

where $k_{material}$ was the thermal conductivity of each layer, A_{cond} was the cross sectional area of conduction, and t was the thickness of each layer. The conduction area applied to the silicon and epoxy was the area of the chip, (10 by 14 mm), while the area applied to the DBC was an average between the chip and the total area of (15 by 17 mm). This resulted in a total resistance of 0.1329 K/W for the stack described by equation 2.4. The 1-D model was used since the size of the sample is comparable to the heater size, so heat spreading would be minimal. The new base temperature was computed using the measured junction temperature, T_j , the applied power, Q , and the thermal resistance, R_{th} , as shown in equation 2.5.

$$T_b = T_j - QR_{th} \quad 2.5$$

In order to calculate an average heat transfer coefficient over the surface it was required to consider an ambient temperature to apply to the surface to compute the temperature difference. Therefore the temperature of the surface of the wick was used since this temperature represents the ambient temperature seen by the water vapor which was escaping from the base of the porous copper as shown in Figure 22 below.

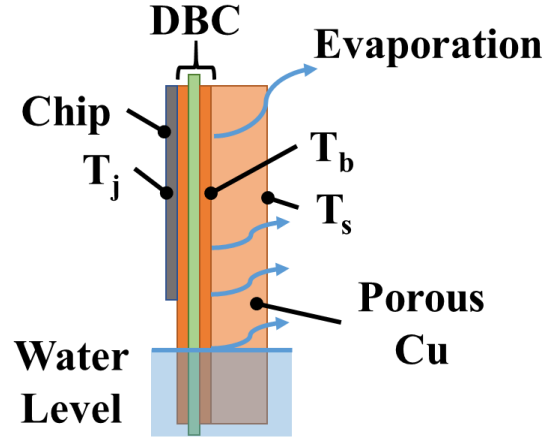


Figure 22. Diagram showing the location of measured temperatures, T_j , T_b , and T_s on the sample, with the vapor escape shown by blue arrows.

The average heat transfer coefficient was then computed with equation 2.6 below using the total outward surface area, (15 by 17 mm), as the area of evaporation, A_{evap} .

$$HTC = \frac{Q}{(T_b - T_s) A_{evap}} \quad 2.6$$

The heat transfer coefficient was plotted as a function of applied power for the 1.138, 0.903, and 0.636 mm wicks as shown below in Figure 23. As shown in the diagram the heat transfer coefficient becomes nearly constant for the 1.138, and 0.636 mm wicks after the onset of boiling where the surface temperature, T_s , reaches $\sim 100^\circ\text{C}$. Unlike the 1.138 mm wick the HTC value of the 0.636 mm wick increased after dry out, implying that even though the measured surface temperature was above 100°C the wick still had not completely dried out.

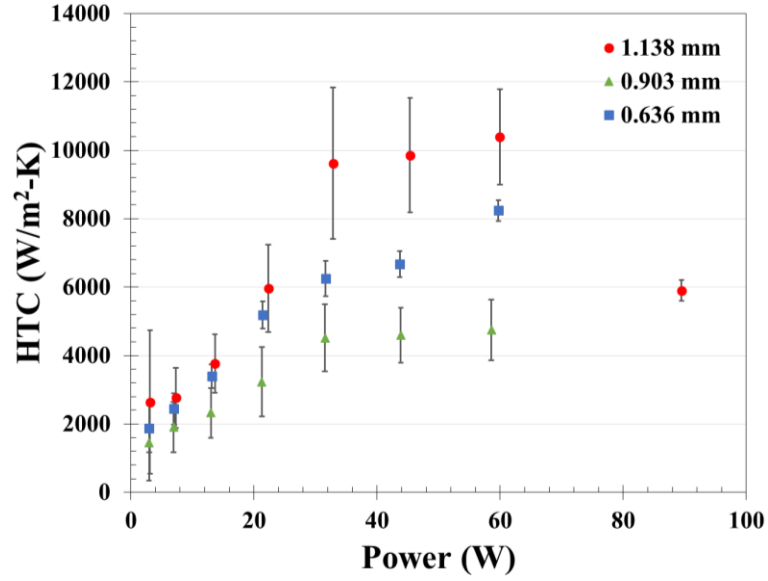


Figure 23. Heat transfer coefficient plotted against the applied power for the 1.138, 0.903, and 0.636 mm wicks showing the dry out of the 1.138 mm wick where the HTC value drops significantly.

Using the estimated base temperature, T_b , and the wick surface temperature, T_s , a boiling curve was produced as shown below in Figure 24. The boiling curve clearly shows that below ~30 W the performance of each was very similar within uncertainty. However as the power was increased nucleate boiling was initiated, as is shown by the increase in slope in Figure 24, and by the measured temperature in Figure 21. In the boiling regime however the thickest wick has a slightly higher heat transfer coefficient, than the other two while the 0.903 mm wick performed the worst.

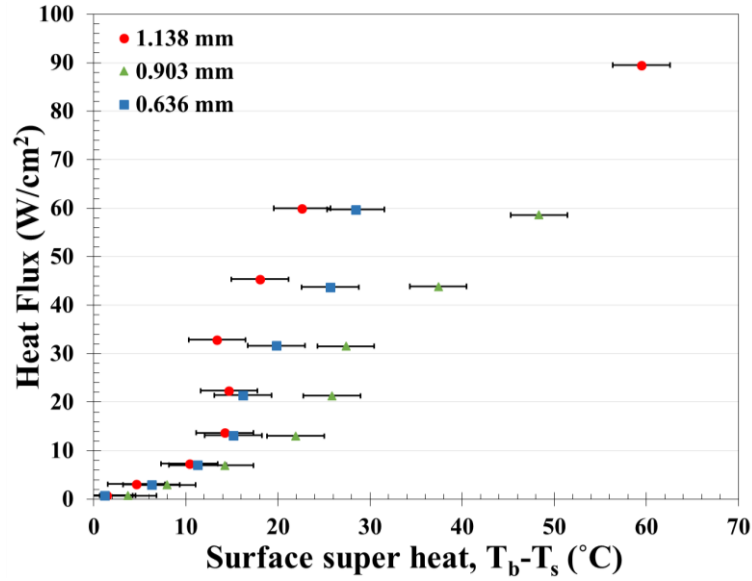


Figure 24. Boiling Curve of the 1.138, 0.903, and 0.603 mm wicks based on the estimated base temperature, and the measured surface temperature.

In order to investigate if the fluid delivery was the cause of surface dry out the capillary performance of the wick was evaluated by balancing the capillary (ΔP_c), viscous (ΔP_v), and gravitational (ΔP_g) pressure drops of the fluid within the wick using equation 2.7, and described by Figure 25. For the capillary pressure to be sufficient to supply fluid to the wick, it must be larger than the viscous pressure and gravitational pressure losses.

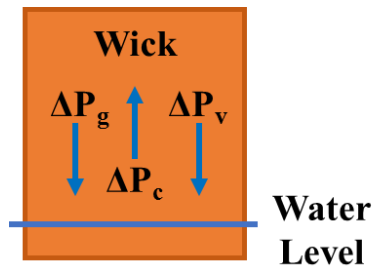


Figure 25. Model showing the capillary pressure which pulls the water up the wick, and the gravitational and viscous pressure which resists the upward flow of water.

$$\Delta P_c > \Delta P_v + \Delta P_g \quad 2.7$$

The above three pressure drops were computed with equations 2.8, 2.9, and 2.10 using water properties taken at the average temperature between the T_w and T_s :

$$\Delta P_c = \frac{2\sigma_l}{r_{eff}} \quad 2.8$$

$$\Delta P_v = \frac{\mu_l H \dot{m}}{\rho_l K A_{wick}} \quad 2.9$$

$$\Delta P_g = \rho_l g H \quad 2.10$$

where σ_l was the surface tension, r_{eff} was the effective particle radius, μ_l was the viscosity, H was the height of the wick, 17 mm, \dot{m} was the mass flow rate, ρ_l was the density, K was the wick permeability, A_{wick} was the cross sectional area of flow in the wick, and g was acceleration due to gravity. The mass flow rate was computed using an energy balance with the applied heat load, and the latent heat, H_v , as shown below in equation 2.11.

$$\dot{m} = \frac{Q}{H_v} \quad 2.11$$

The effective radius, r_{eff} was computed from equation 2.12 using the average particle diameter D , (9.57 μm), [87].

$$r_{eff} = 0.21D \quad 2.12$$

The permeability of the wick was computed using a correlation for irregularly shaped particles given by Garcia et al. [88] in equation 2.13 where ε was the porosity of the wick taken from Table 3.

$$K = 0.11D^2 \varepsilon^{5.6} \quad 2.13$$

By applying a mass conservation to the wick the fluid velocity at the inlet was computed using equation 2.14.

$$v_f = \frac{\dot{m}}{\rho_l A_{wick}} \quad 2.14$$

The total pressure was computed by subtracting the gravitational and viscous pressure drops from the capillary pressure, and was plotted below for all three wick thicknesses in Figure 26.

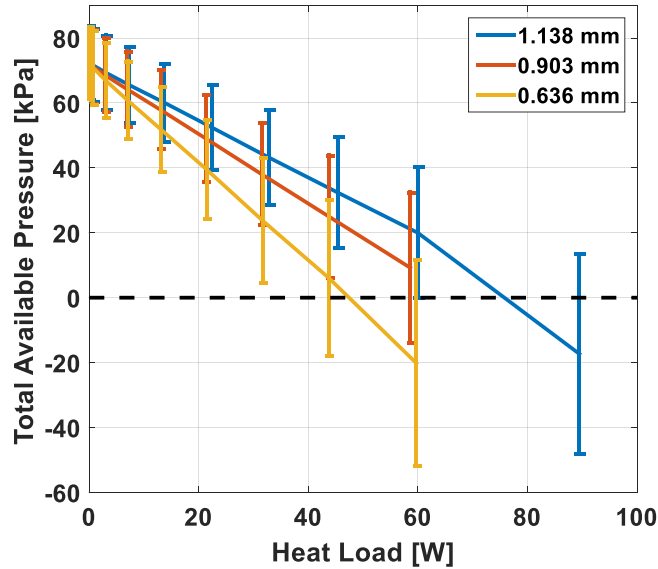


Figure 26. Total pressure computed for the 1.138, 0.903, and 0.636 mm thick wicks as a function of applied power with uncertainty bounds, and the point of dry out shown by where the available pressure drops below the dotted line.

Above a certain power level Figure 26 shows that the total pressure does in fact become negative, within the bounds of uncertainty. This supports the possibility that the limiting factor of the wick performance was the ability of the wick to deliver fluid to the evaporative

area. This same principal can also be seen by plotting the required fluid velocity computed by equation 2.14, and comparing it to the velocity of the fluid estimated using the applied capillary pressure as shown in equation 2.15.

$$v_{\Delta P} = \frac{(\Delta P_c - \Delta P_g)K}{H \mu_l} \quad 2.15$$

As evident by Figure 27, within uncertainty bounds the fluid required by the mass balance was larger than the fluid velocity that is possible with the given capillary pressure.

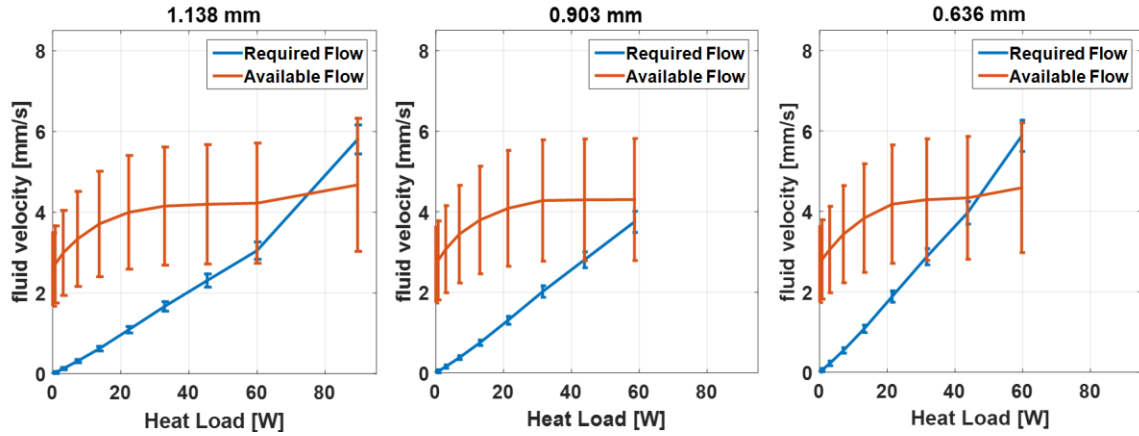


Figure 27. Fluid velocity required by mass conservation plotted in blue compared to maximum fluid velocity possible due to capillary pressure.

The fluid velocity due to equation 2.14 increased above the lower bound of $v_{\Delta P}$ around 70 W for the 1.138 mm sample, just over 40 W for the 0.903 mm sample and just under 40 W for the 0.636 mm sample. This shows that the dry out for each sample could have been due to the lack of pressure required to overcome the viscous pressure as the actual dry out powers were above these lower limits. The large error bars on Figure 27 were primarily due to the uncertainty in the permeability due to uncertainty in particle size. The uncertainty in porosity was only $\pm 0.4\%$, giving a relative uncertainty of only 0.6%, however the relative

uncertainty of the particle size was 15.8% leading to a relative uncertainty in permeability to be 31.4% as shown by equation 2.16. Since the relative uncertainty in particle size was multiplied by 2, due to propagation of error shown by equation 2.13, the relative uncertainty in permeability was significantly increased:

$$\frac{U(K)}{K} = \sqrt{\left(\frac{2U(D)}{D}\right)^2 + \left(\frac{5.6U(\varepsilon)}{\varepsilon}\right)^2} \quad 2.16$$

where $U(A)$ is the uncertainty in the variable in the parenthesis, and all other variables have been previously defined. Since the large uncertainty creates difficulty in seeing the differences in performance due to design parameters a parametric study was conducted. The capillary pumping model was used to investigate the expected changes in performance due to changes in design parameters such as porosity, particle size, wick thickness, and operational parameters such as heat load and inlet water temperature.

2.5.2 Parametric study of wick thickness

In order to investigate the expected differences in capillary pumping performance due to changes in the different design parameters the pressure model was applied with changing fluid temperatures, porosities, and particle sizes. Since the experiments were performed with water below the saturation temperature the effect of different inlet temperatures was investigated first. Due to the higher water viscosity at lower temperatures the viscous pressure losses were much higher at temperatures below ~40°C as shown in Figure 28 below.

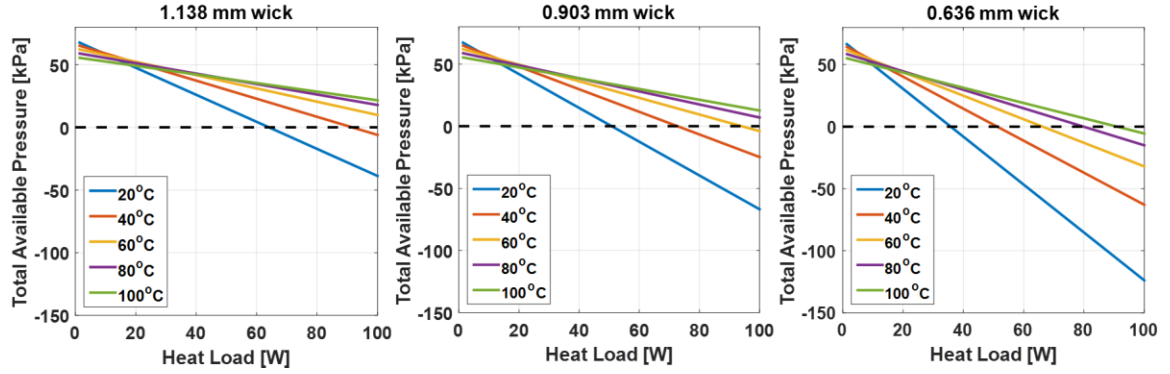


Figure 28. Effect of water temperature on available capillary pressure for wicking, and showing the estimated point of dry out when the available pressure falls below zero as indicated by the dotted line.

For the 1.138, and 0.903 mm wick the estimated dry out power was increased from ~50 W, to over 100 W by increasing the temperature from 20°C to 100°C. For the 0.636 mm wick dry out increased from <40 W up to 100 W, showing that the smaller wick was much more affected by the fluid temperature due to the smaller cross sectional area for fluid travel. Since the best pumping performance was at the highest temperature, and the worst was at the lowest, the three different wick thicknesses were compared at these two temperatures in Figure 29 to show the range of pumping performance.

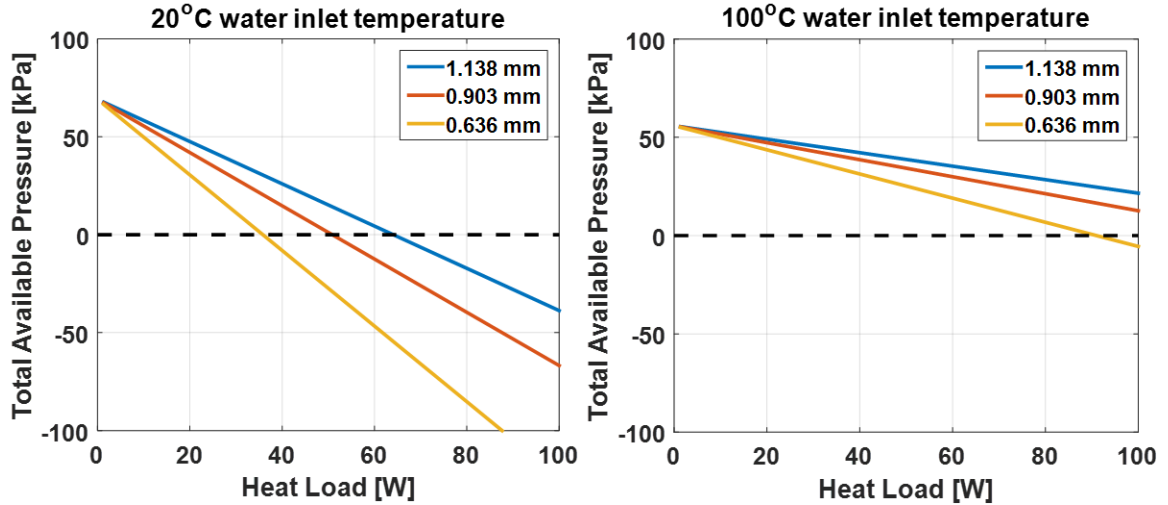


Figure 29. Plots showing the effect of increasing the wick thickness on the available pumping pressure at 20°C, and 100°C with dry out indicated by the dotted line where the available pressure goes below zero.

With an inlet temperature of 20°C, increasing the thickness of the wick increased the dry out power from <40 W to ~65 W. However with an inlet temperature of 100°C the model suggests the dry out limit of the thinnest wick would be ~100 W and the thickest could be significantly higher.

To evaluate the effect of porosity on the pumping performance the model was run with a particle size of 10 μm , a water inlet temperature of 60°C, wick thicknesses of 1.138, 0.903, and 0.636 mm, and five different porosities as shown in Figure 30. Increasing the porosity by only 0.05 significantly increased the available pumping pressure, increasing the dry out heat load by more than 20 W for each wick. This shows that the porosity was one of the most significant factors in wick dry out. Since the wick was made of irregularly shaped particles with a large uncertainty in size, the porosity also could vary across different parts of the wick. This effect could cause choke points within the wick that reduce the effective water flow area, adding variability to the experimental results.

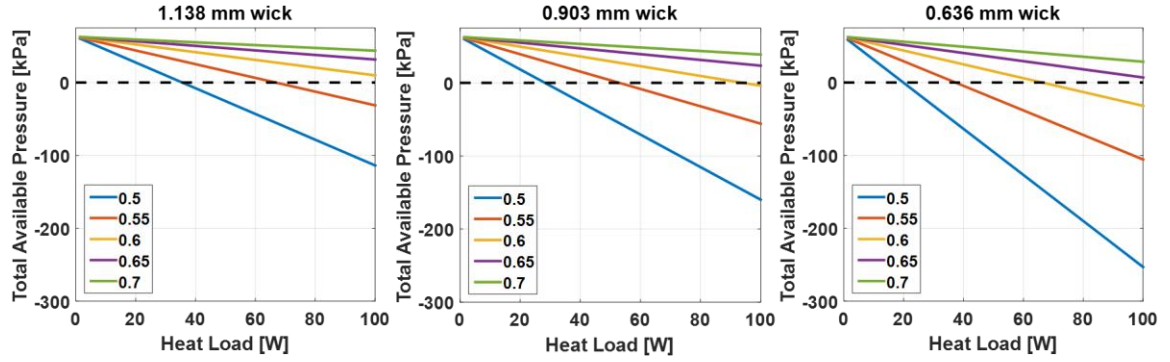


Figure 30. Plot showing the effect of porosity on performance of the 1.138, 0.903, and 0.636 mm wick using water at 60°C, a particle size of 10 μm and with porosities of 0.5, 0.55, 0.6, 0.65, and 0.7.

Finally to investigate the effect of particle size on the pumping performance of the wick model the particle diameter was changed ranging from 5 to 100 μm as shown in the Figure 31 below. In this model the wick thicknesses of 1.138, 0.903, and 0.636 mm were used with water properties taken at 60°C, and a porosity of 0.6 to plot the available pumping pressure.

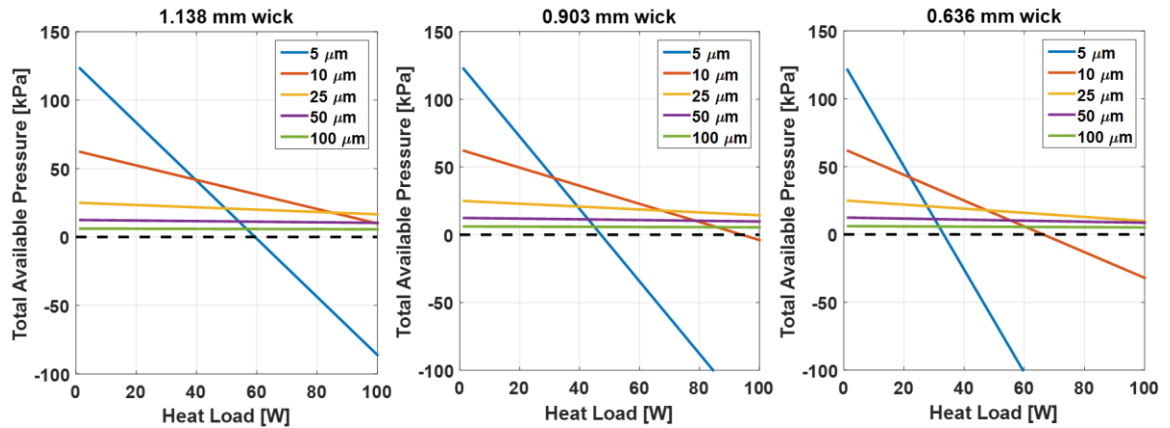


Figure 31. Plot showing the pumping performance of the 1.138, 0.903, and 0.636 mm thick wick, at 60°C water temperature, with a porosity of 0.6 and with particle diameters of 5, 10, 25, 50, and 100 μm .

Reducing the particle size to 5 μm lead to a significant reduction in the available pressure at heat loads above 30-60 W. This was due to the fact that decreasing the particle size increases the capillary pressure by $1/D$ as shown by equation 2.8, however it increases the viscous resistance by a factor of $1/D^2$ as show by equations 2.9, and 2.13. However at low heat loads where the mass flow rate was low, the available pressure was much higher. Increasing the particle size larger than 25 μm also seemed to have very little effect on the dry out heat load within the 100 W experimental range, and only served to decrease the available pressure. This implies that another possible cause of local surface variability could be caused by a conglomerate of small particles within the irregular bed. This effect shows that the expected heat load should be a factor in determining the particle size to use in an evaporative cooler, as smaller particle sizes will give better pumping performance at low heat loads.

2.5.3 *Effect of wick width*

A similar analysis was performed on the large area wicks in order to determine the performance and the cause of dry out. The total thermal resistance for these samples was also computed with equation 2.2, and displayed below in Figure 32. In the low power regime, (below about ~15 W), the uncertainty was very large due to the uncertainty in ($T_j - T_w$) being of the same order of magnitude to the actual temperature difference. Above that range the uncertainty reduced significantly, and it can be seen that the 25 mm sample had a slightly higher thermal resistance than the other two samples.

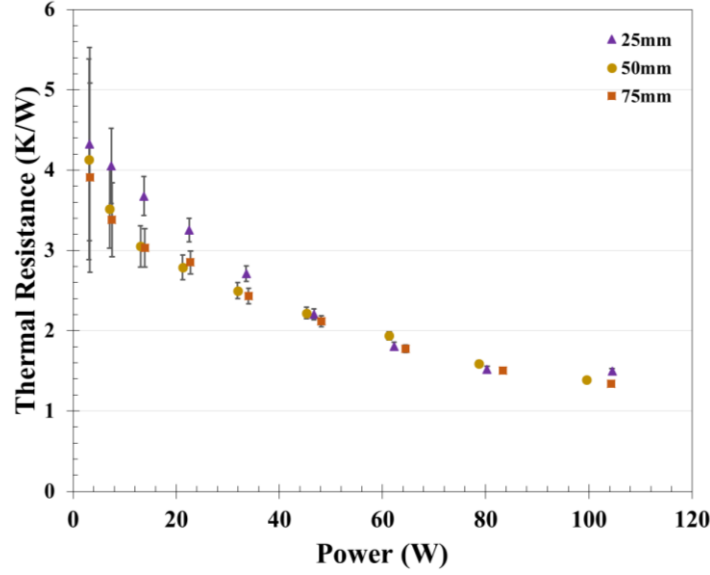


Figure 32. Thermal Resistance of the 25, 50, and 75 mm sample widths plotted against the applied power.

However, after ~40 W of power was applied the thermal resistance of all three samples became very similar. This behavior was presumed to be due to the change in heat transfer mechanism from evaporation to boiling around 40 W. This transition was known because the central surface temperature at 33.6 W for the 25 mm sample was 91.2°C, and at 46.7 W, the temperature became 98.4°C, around boiling temperature at ambient pressure. In the evaporation regime the mass flux out of a surface behaves according to the Hertz-Knudsen equation, (2.17), shown below:

$$m'' = \gamma \sqrt{\frac{M}{2\pi R}} \left(\frac{P_v}{\sqrt{T_v}} - \frac{P_a}{\sqrt{T_a}} \right) \quad 2.17$$

where m'' is the mass flux, γ is an evaporation coefficient between 0 and 1, M is the molar mass of the liquid evaporating, R is the universal gas constant, P_v is the pressure of the escaping vapor, P_a is the partial pressure of the liquid in the ambient air, T_v is the

temperature of the escaping vapor, and T_a is the temperature of the ambient environment. Since the term $P_v/\sqrt{T_v}$ increases exponentially with temperature the mass flux also follows this trend as all other terms remain constant. This implies that in the purely evaporative regime, the larger surface area of the 50 and 75 mm samples is able to provide noticeably more heat transfer, and thus lower thermal resistance. However, once boiling begins the evaporation away from the center does not provide appreciable heat transfer as compared to the nucleate boiling within the central area.

In order to further investigate possible performance limits of the wicks, the applied heat flux was plotted against the surface super heat for all three wicks as shown in Figure 33 below.

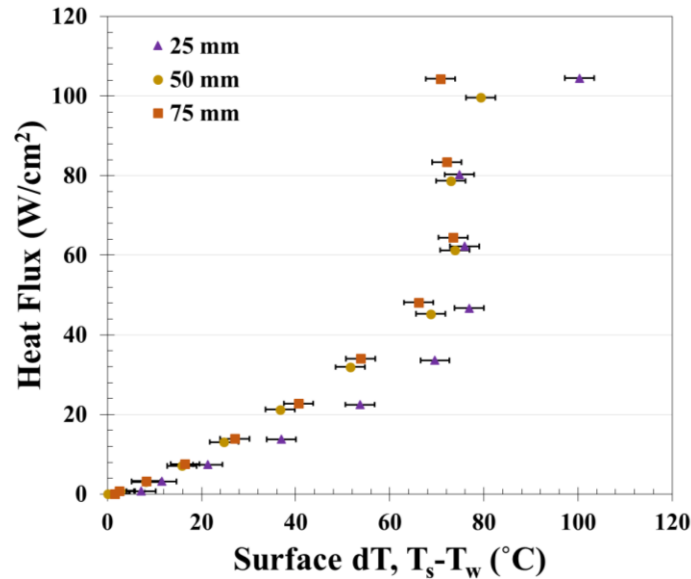


Figure 33. Plot of applied heat flux vs. the difference in the surface and water temperature for the 25, 50, and 75 mm wide wicks, showing the point when surface dry out began to take place.

Similar to the 15 by 17 mm wicks the surface super heat remains constant once boiling begins, and eventually a point was reached where the surface dries out and the temperature

significantly increased. This result was also consistent with a similar study of sintered copper mesh surfaces by Chen Li et al. which found a transition to boiling around 25 W [89]. In the study by Chen Li the sintered copper mesh was 8 mm wide, and extended 152.4 mm long, with a wire diameter of 56 μm , so it was comparable to the scale of this current study. However, the limit reached was much higher for these samples, and the increase in temperature was much smaller. The 25 and 50 mm samples both reached dry out after ~80 W was applied, however the temperature increase for the 25 mm was much larger than for the 50 mm. The 75 mm sample was not able to attain dry out within the 100 W power limit of the 2425 Kiethley Source Meter that was used. By plotting the boiling curve for all temperature locations on the 75 mm sample in Figure 34 it was also confirmed that the primary heat transfer/evaporation took place in the central region.

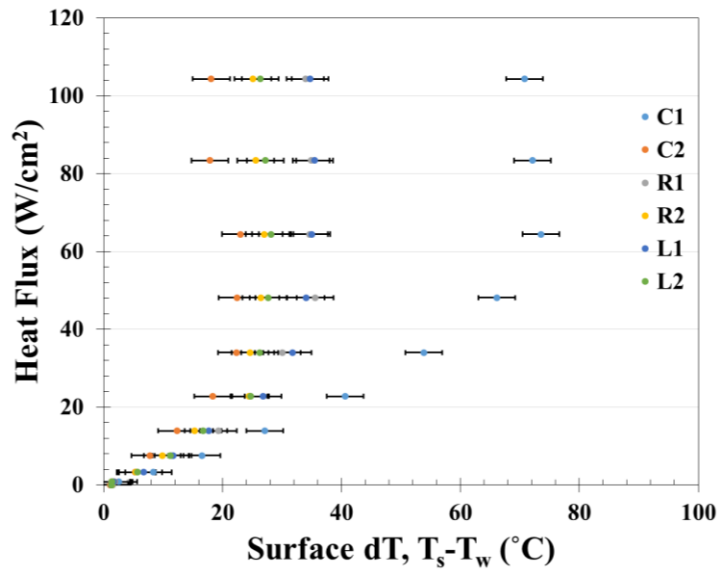


Figure 34. Plot of applied heat flux vs. the difference in the surface and water temperature for the 75 mm sample showing the point when surface dry out began to take place. The locations of C1, C2, R1, R2, L1, and L2 are shown below in Figure 35.

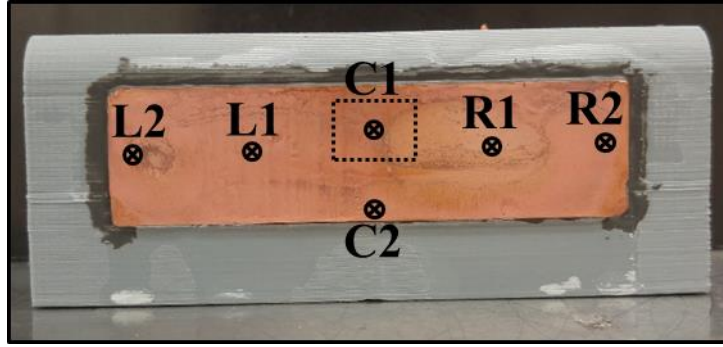


Figure 35. Picture of 75 mm sample labeling the locations where the temperatures were measured, and a dotted line indicating the location of the heater.

From Figure 34, it can be clearly seen that the surface temperature outside of a ~20 mm radius from the center was significantly smaller than the temperature at location C1. Similar to the smaller wicks, according to the Hertz-Knudsen equation, 2.17, the evaporative mass flux, and thus heat transfer, was also significantly smaller in the outer regions. Thus, it shows that the primary reason for the similar thermal resistances of the wicks is that the central area is the only place where significant heat transfer occurs, but the heat load limits are affected by the wick structure.

In order to investigate the effect of wick structure on dry out the capillary performance of the wick was modeled. However, for the larger wicks a different model for fluid flow had to be adapted. The reason was that with a central heat source all the fluid was not approaching the evaporative area along the same path as shown in Figure 36, as water coming from the edge must travel further than water from directly below.

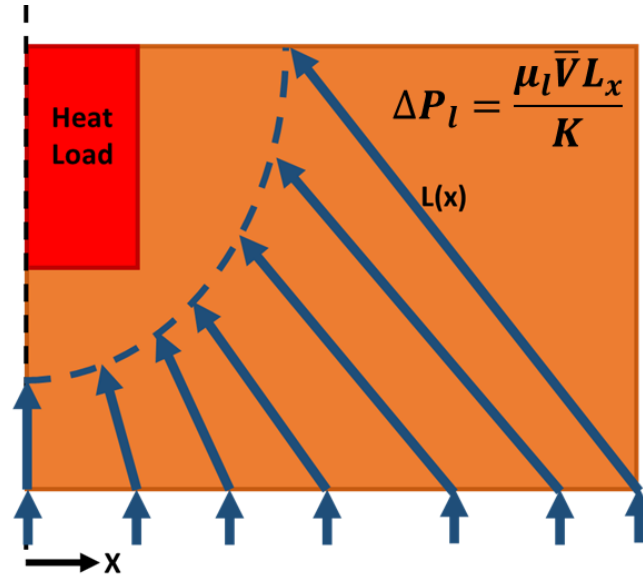


Figure 36. Fluid flow model applied to the 25, 50, and 75 mm wicks in order to estimate the total pressure losses to transport fluid from the base to the central evaporative/boiling area.

Therefore, the viscous pressure drop was not able to be easily computed from the simple height of the wick. This problem was solved numerically with a distributed mass flow model shown in Figure 37 assuming that the pressure difference between any two base locations and the central heat source was the same.

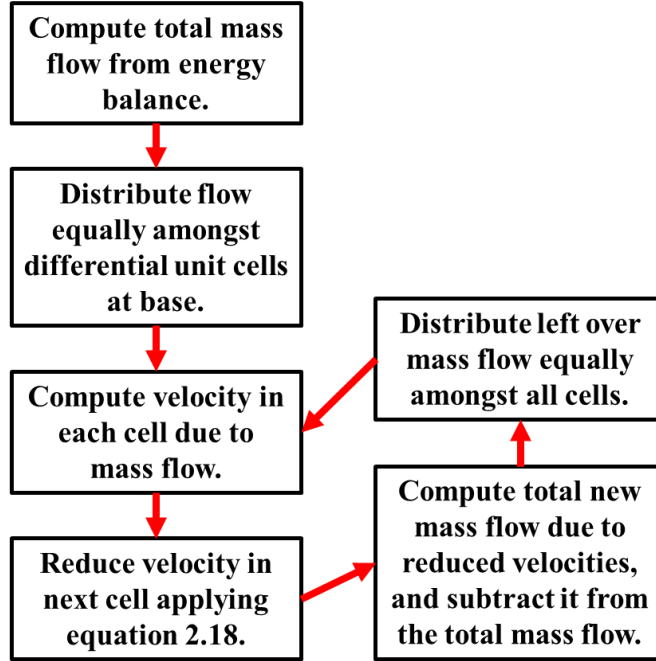


Figure 37. Iterative process used to compute the mass flow distribution, using a convergence criterion as the point when the largest difference between any two viscous pressures along the base was less than 0.01% of the smallest pressure drop.

This model was developed using the ratio of the velocities computed for viscous flow through two different paths to the center as shown by equation 2.18:

$$\frac{v_i}{v_{i+1}} = \frac{\sqrt{x_i^2 + L^2}}{\sqrt{x_{i+1}^2 + L^2}} \quad 2.18$$

where v_i and v_{i+1} were the velocity at positions x_i and x_{i+1} respectively, and L was the height of the sample. Since velocity was reduced along the base, this guaranteed that the model could not overshoot the applied mass flow rate. A representative mass flow rate distribution is shown below for the 75 mm sample at ~100 W in Figure 38, and it can be seen that as expected most of the flow occurs at the center with less coming from the edges of the sample.

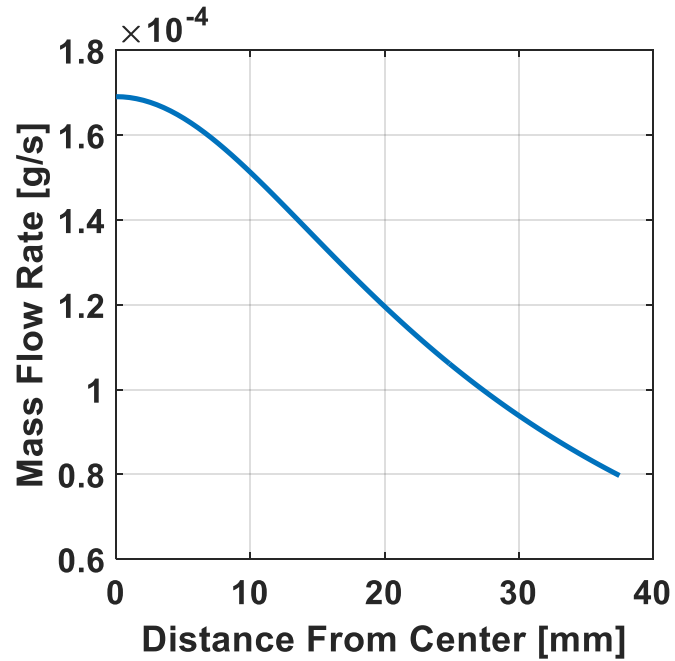


Figure 38. Mass Flow Rate distribution across the base of the 75 mm sample with ~100 W of heat applied computed using the iterative model described by Figure 37.

Applying these mass flow rates to equation 2.9, the pressure drop from any point along the base to the top center of the wick was estimated, and the minimum value was plotted below in Figure 39. Although the uncertainty in the pressure calculation was too large to differentiate the three samples significantly, they all show that the total available pressure was still larger than zero, implying total surface dry out would not occur.

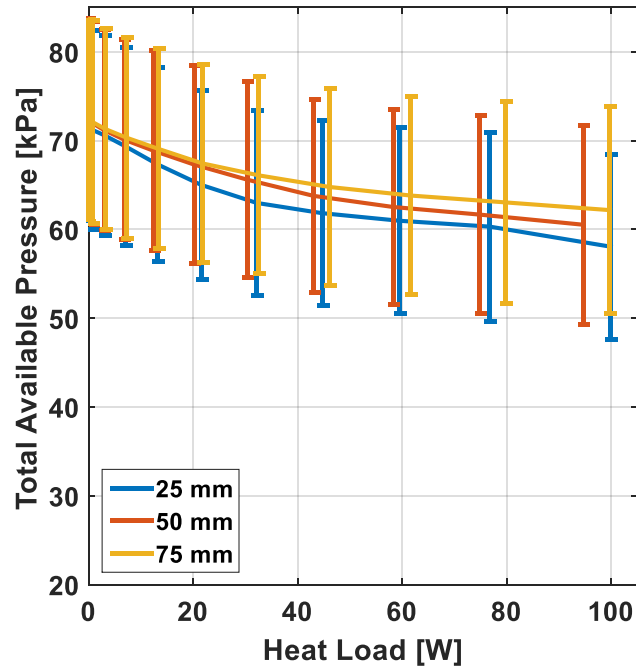


Figure 39. Total available pressure computed by subtracting the viscous, and gravitational pressure drop from the available capillary pressure.

Although the model predicts that none of the wicks would reach dry out, the 25 and 50 mm samples did. This was most likely because constriction pressure was not included in the simplified pressure model. As the fluid approaches a single point the available cross sectional area reduces, causing an increase in velocity and thus increase in viscous pressure. However this model was still able to show that dry out of the entire sample will not occur, although localized dry out was possible. Since the behavior of all three wicks was similar within uncertainty in the model it would have also been expected that the local dry out should have also occurred at similar powers. This implies two possible explanations, one that the larger samples had lower constriction pressures. The second possible explanation is that the increased heat spreading of the larger sample reduced the heat load at the center enough that less mass flow was required there, reducing the constriction pressure. Since the large uncertainty makes it difficult to evaluate the differences in performance due to

design parameters a parametric study was conducted. The large area capillary pumping model was used to investigate the expected changes in performance due to changes in design parameters such as porosity, particle size, wick width, and operational parameters such as heat load and inlet water temperature.

2.5.4 Parametric study of wick width

In order to investigate the expected differences in capillary pumping performance due to changes in the different design parameters the modified pressure model was applied with changing fluid temperatures, porosities, and particle sizes. Since the experiments were performed with water below the saturation temperature the effect of different inlet temperatures was investigated first. The results of this are shown below in Figure 40, and it can be seen that for the 25 mm wick the dry out heat load is only reached for the 20°C water temperature, at >80 W of power. For the 50 and 75 mm wide wicks the dry out was not reached for any temperature within the 100 W experimental range that was investigated. This implies that the large area wicks are more suitable for subcooled evaporation where high viscosity can significantly affect the viscous pressure losses.

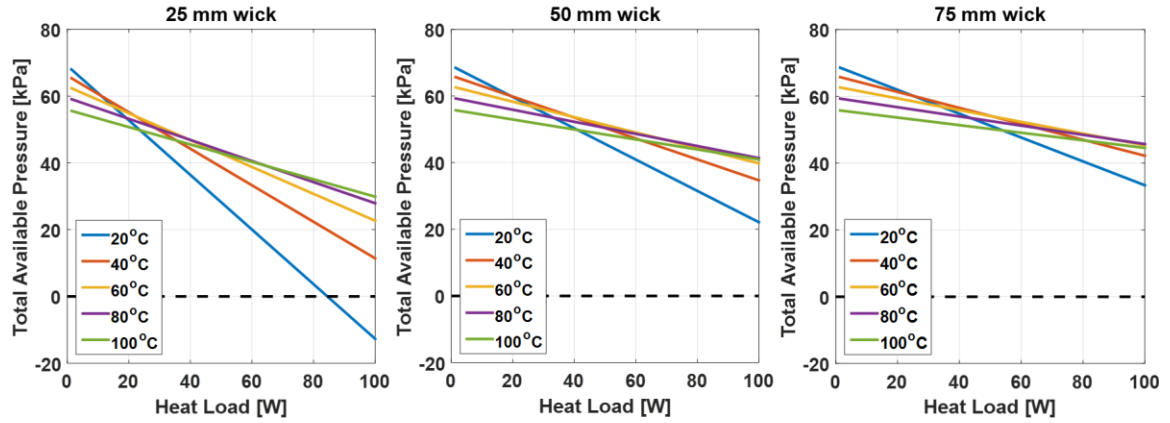


Figure 40. Plots showing the effect of inlet water temperature on the pumping performance of the 25, 50, and 75 mm wide wicks with the dry out indicated by when the pressure curves drop below the dotted line.

The effect of wick width was then compared at 20°C, and 100°C since this represents the upper and lower limits of the model. As can be seen in Figure 41 increasing the width of the sample from 25 mm to 50 mm significantly increased the available pressure by more than 30 kPa with 20°C inlet water temperature, and more than 10 kPa at 100°C inlet temperature. However increasing the width further to 75 mm only increased the pumping pressure by about a third of the previous increase, at both temperatures.

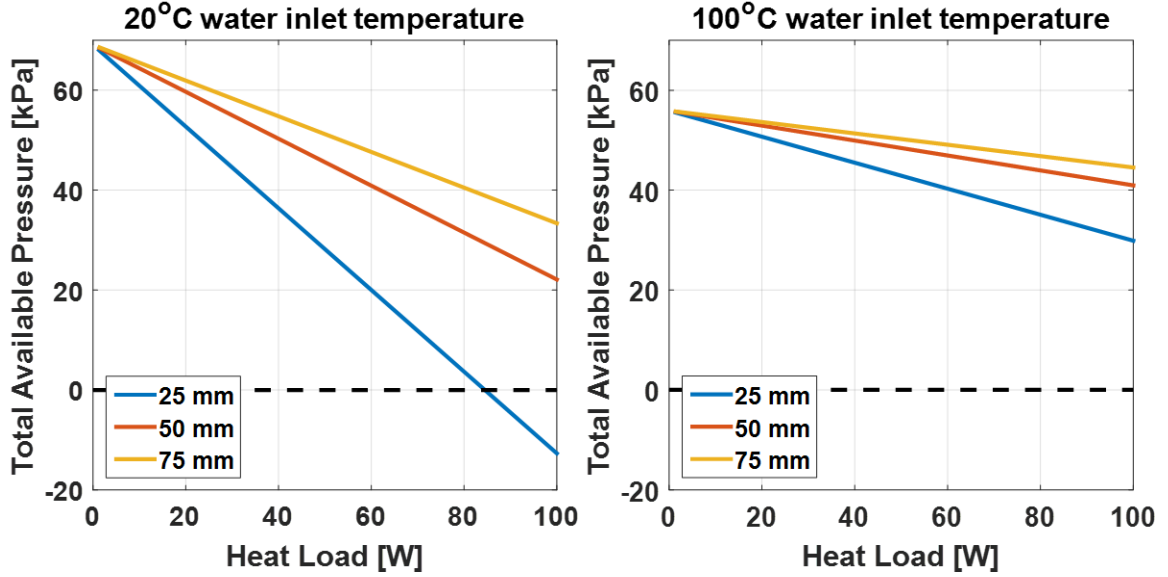


Figure 41. Plots showing the pumping performance of the 25, 50, and 75 mm wicks at 20°C, and 100°C with the dry out heat load shown by the point where the pressure curve goes below the dotted line.

To evaluate the effect of porosity on the model behavior the model was run at 60°C inlet water temperature, with a particle size of 10 μm , and porosities of 0.5, 0.55, 0.6, 0.65, and 0.7. The results are shown below in Figure 42 comparing the relative effects of porosity changes for the three different wick widths.

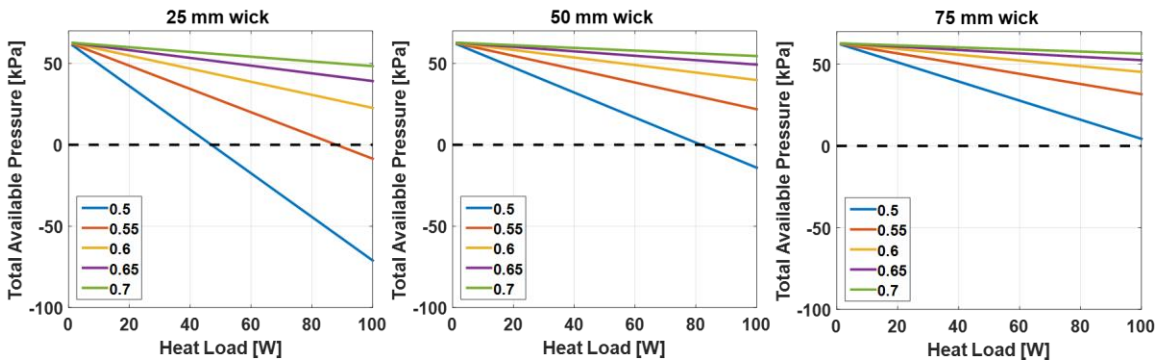


Figure 42. Plots showing the effect of porosity on the pumping performance of the 25, 50, and 75 mm wicks with a water inlet temperature of 60°C, and a particle diameter of 10 μm , with the dry out shown by the place where the pressure goes below the dotted line.

Similar to the effect of wick thickness, increasing the porosity significantly increased the available pumping pressure at high power levels. However at low power levels the pumping pressure was comparable across the different wicks. As expected increasing the wick width from 25 to 50 mm increased the pumping pressure, much more than increasing the pumping pressure from 50 to 75 mm.

The effect of particle size was investigated for the three wicks with an inlet water temperature of 60°C, and a porosity of 0.6 as shown in Figure 43 below. Increasing the particle size above 25 μm only served to decrease the available pressure, but did not affect the dry out limit within the 100 W range. This effect was also almost identical across the different wick thicknesses, although decreasing the particle size to 5 μm significantly reduced the available pressure at high power levels for the 25 mm wick.

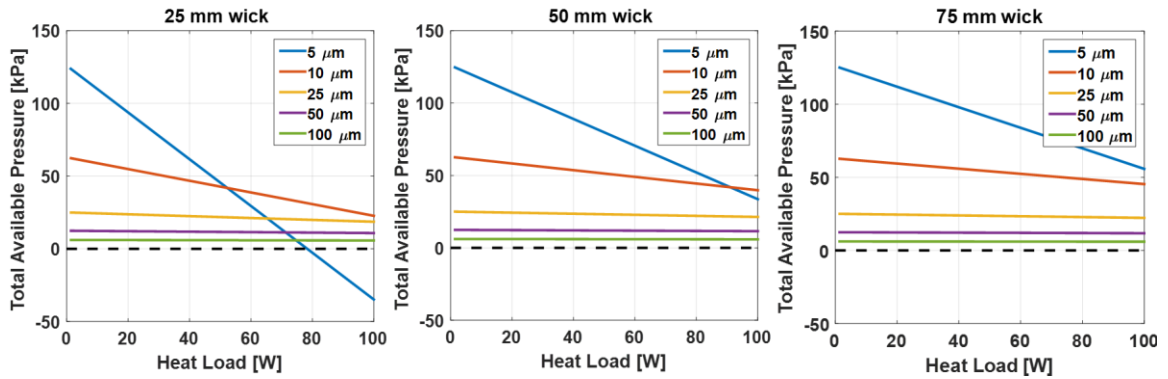


Figure 43. Plots showing the effect of changing the particle size on the pumping pressure of the 25, 50, and 75 mm width wicks with an applied inlet water temperature of 60°C, and porosity of 0.6. The particle diameters applied to the model were 5, 10, 25, 50, and 100 μm .

2.5.5 Boiling Limit

The parametric studies on the thickness and width of the capillary wicks were able to show that the wicks can very easily be designed to handle extremely high heat loads while still having enough capillary pressure to maintain fluid in the wick. However, despite the pumping ability of the wick, if nucleate boiling initiates, escaping bubbles can fill the wick and block incoming liquid. A conservative estimate for the critical surface super heat is based on the nucleation radius, and available capillary pressure and given by equation 2.19 , [90]:

$$\Delta T_c = \frac{T_{sat}}{H_v \rho_v} \left(\frac{2\sigma_l}{r_n} - \frac{2\sigma_l}{r_{eff}} \right) \quad 2.19$$

where ΔT_c is the critical surface super heat, T_{sat} is the saturation temperature, and r_n is the nucleation radius. As the wall super heat is shown by equation 2.19 to be very sensitive to r_n , and r_{eff} Figure 44 was plotted below to show the effect of both parameters on the critical surface super heat.

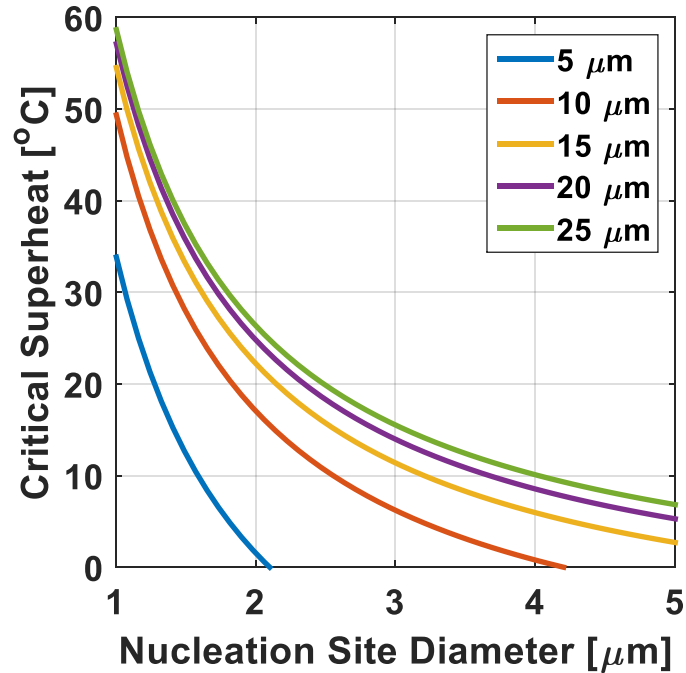


Figure 44. Critical surface superheat plotted as a function of nucleation site diameter for 5, 10, 15, 20, and 25 μm particle diameters.

Experimentally the transition to boiling occurred between approximately 10°C and 30°C, corresponding to a nucleation site size between 1.5 and 2.5 μm on the 10 μm particle diameter curve. By looking at Figure 12 which shows SEM images of the sintered copper particles it can be seen that there are particles within the range of the nucleation site size. This means that the dry out limit which was reached experimentally for the 25, 50, and 75 mm wide samples was not a capillary limit, but a boiling limit. Although the wick has sufficient capillary pressure to pump the fluid, the bubble nucleation was blocking rewetting of the dry surface.

2.5.6 Comparison to Standard IGBT Packaging

In order to estimate the potential gain by integrating this cooling technology into DBC instead of after a heat spreader a comparative study was performed in ANSYS. In

this study, a representative IGBT module was designed, based on the ABB HiPak module with 6 integrated IGBTs [91]. In order to reduce computational time of the model the system was reduced to a single unit cell of the HiPak module as shown below in Figure 45. The location of the heat load and convective boundary condition are shown in Figure 46 for the baseplate module, and the integrated cooling module.

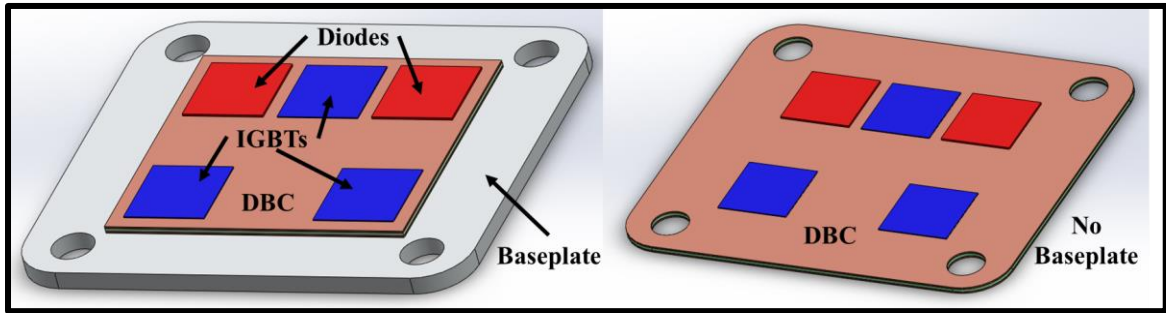


Figure 45. Single unit cell of ABB HiPak IGBT inverter module showing the IGBTs in blue, with the diodes in red. The chips sit on a DBC substrate with a 3 mm baseplate (Left), and without a baseplate for the integrated model (Right).

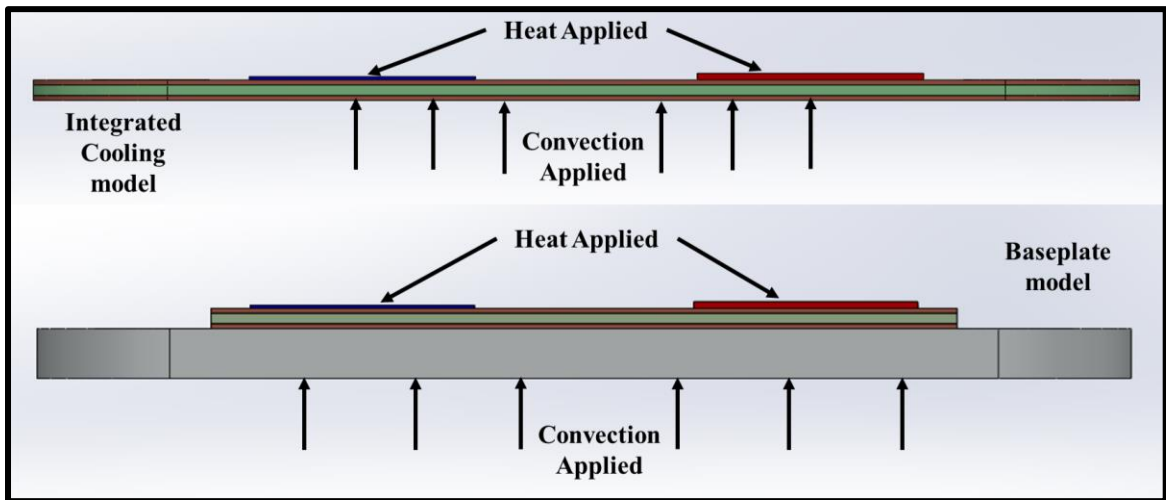


Figure 46. Diagram showing the location of the applied heat load and convective boundary on the integrated cooling model, (top), and the baseplate model, (bottom).

The DBC was comprised of an AlN layer with two copper metallization layers on each side, while the IGBTs and diodes were given the properties of silicon. The Au-Sn solder between the chips and the DBC, and DBC and AlSiC was modeled as a thermal interface conductance of $0.877 \text{ K-m}^2/\text{MW}$ computed from the thermal conductivity and layer thickness given in Table 5 below.

Table 5. Thermal properties and thicknesses of materials used in numerical model.

Material	Thermal Conductivity (W/m-K)	Thickness (μm)
Silicon	130	190 (IGBT), 390 (Diode)
Au-Sn Solder	57	50
Copper	385	300
AlN	157	630
AlSiC	185	3000

The heat applied to the IGBTs and the diodes was split 85.7% to the IGBTs, and 14.2% to the diodes. This power split estimate was based on modeling by Narumachi et al. which was performed on an inverter for a Toyota Prius [28]. A parametric study was performed with all combinations of the heat loads, fluid temperatures, and heat transfer coefficients shown in Table 6 below.

Table 6. Parameters changed during numerical modeling of the IGBT.

Fluid Temperature ($^{\circ}\text{C}$)	Heat Load (W)	Heat Transfer Coefficient ($\text{W/m}^2\text{-K}$)
50	100	5,000
100	300	15,000
-	500	50,000
-	700	100,000

In order to ensure the results were independent of the mesh size, a mesh independence study was performed. The mesh independence was performed with 100 W of power

applied, and 5,000 W/m²-K heat transfer coefficient applied to the base. The mesh was refined until the maximum temperature changed by less than 2%, as shown below in Figure 47.

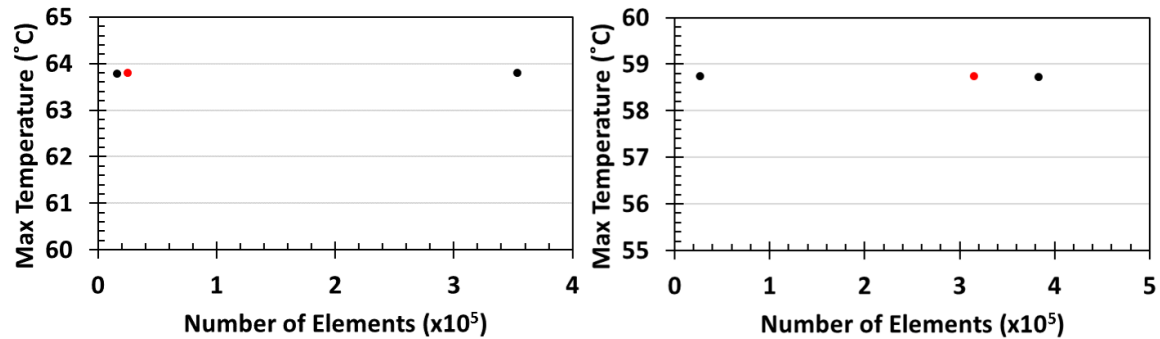


Figure 47. Change in maximum temperature as the number of elements in the mesh was increased, showing the integrated model (Left), and the baseplate model (Right). The mesh size used for further modeling was indicated by the red marker.

This numerical model was used as a baseline for comparison, and was modified by removing the baseplate and applying the HTC values directly to the back side of the DBC to compare to the integrated cooling method. Then the material of the AlSiC plate was changed to be copper to consider a high thermal conductivity heat spreader as well. The maximum temperature on the model, indicated in Figure 48, was plotted as a function of heat transfer coefficient for different applied heat loads, and ambient temperatures below in Figure 49. The maximum temperature was always found on the bottom center IGBT chip since the bottom center chip always had the least space available around it for heat spreading, as it was surrounded by two diodes.

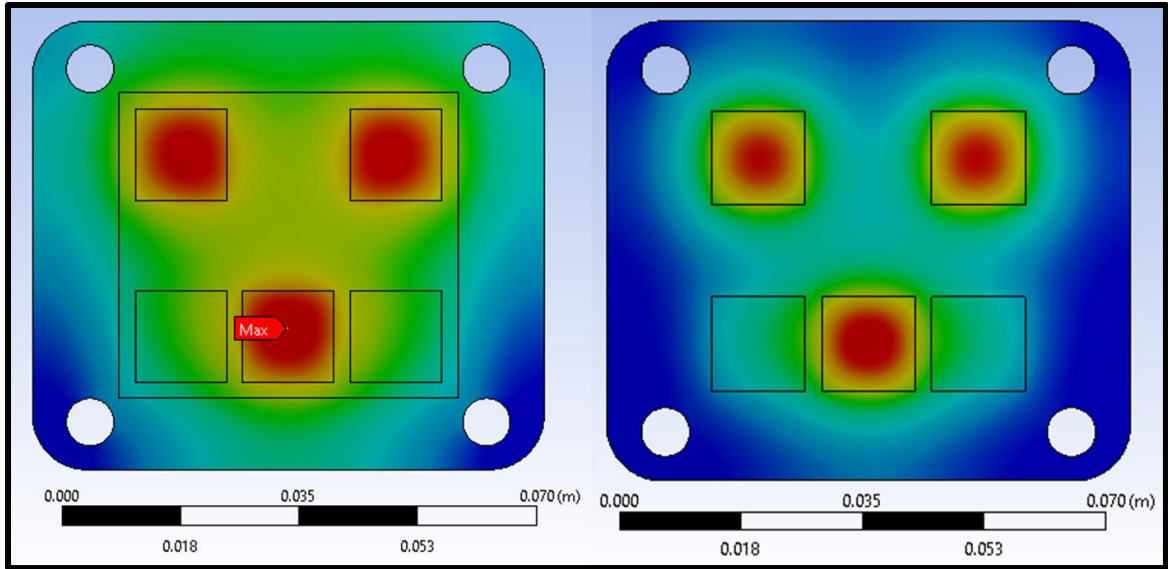


Figure 48. A typical temperature distribution of the IGBT module showing the baseplate model (Left), and the integrated cooling model (Right) with the location of the maximum temperature on the model with a red flag.

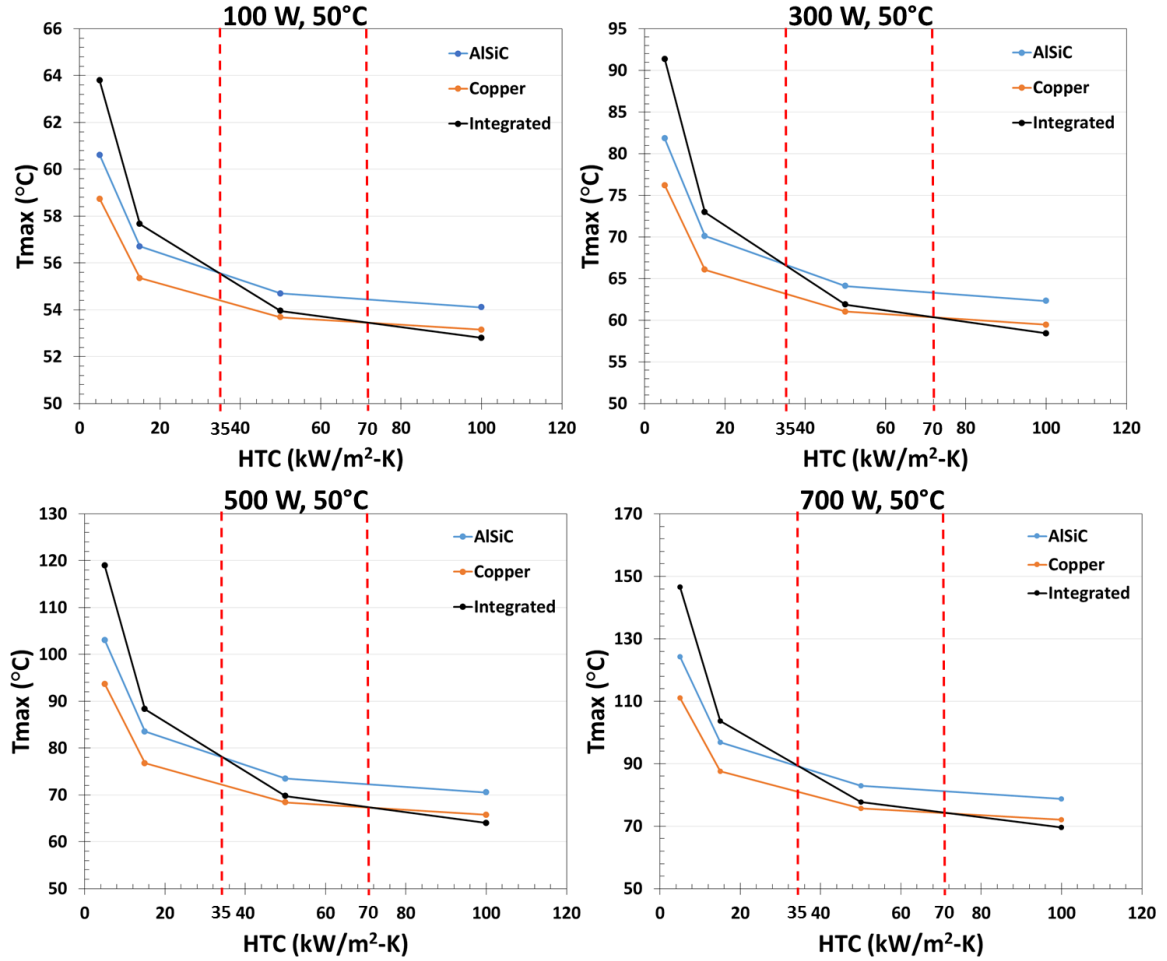


Figure 49. Maximum temperature plotted against heat transfer coefficient for 100 W (Top Left), 300 W (Top Right), 500 W (Bottom Right), and 700 W (Bottom Left) applied heat loads at 50°C ambient temperature. The HTC values where the integrated cooling becomes better than the AlSiC, and copper baseplates are shown with dotted red lines.

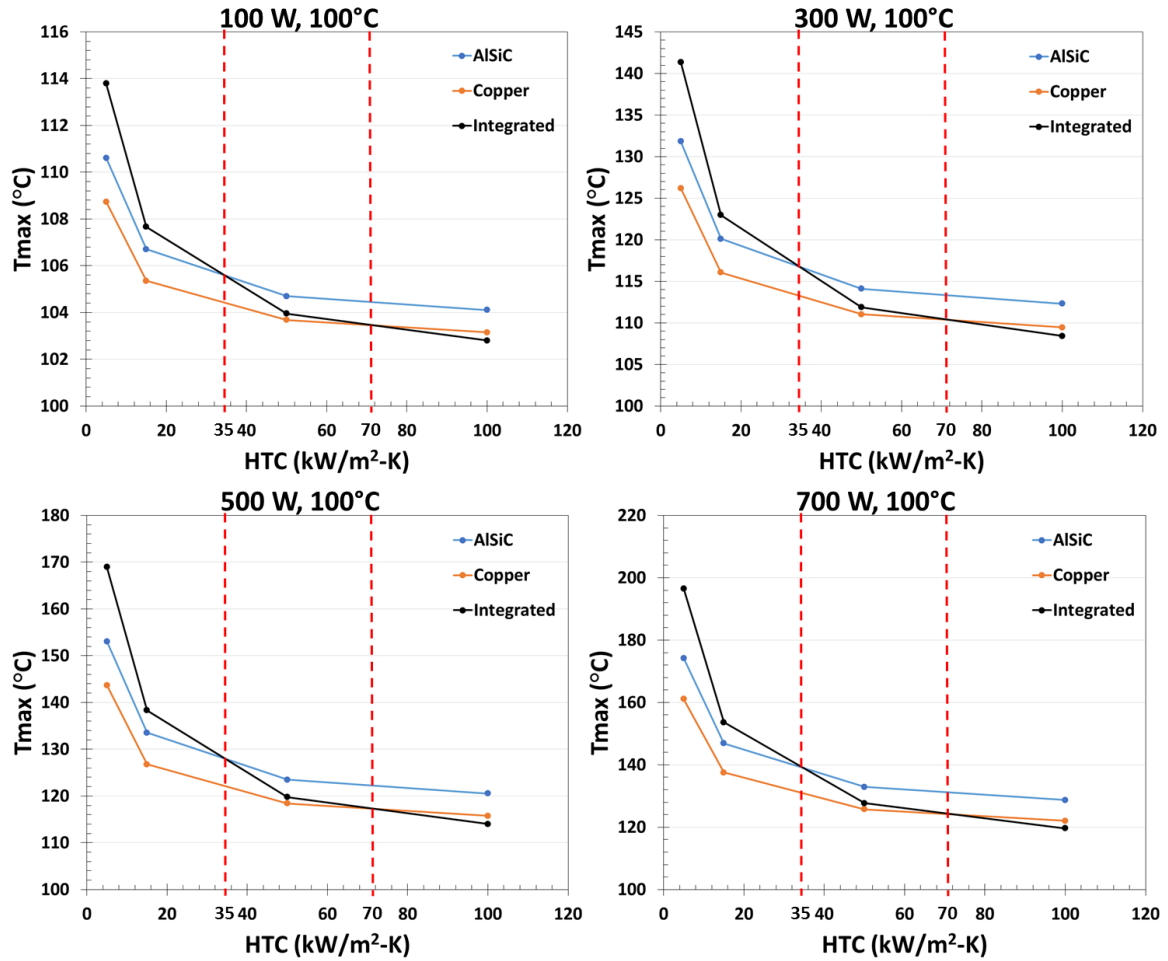


Figure 50. Maximum temperature plotted against heat transfer coefficient for 100 W (Top Left), 300 W (Top Right), 500 W (Bottom Right), and 700 W (Bottom Left) applied heat loads at 100°C ambient temperature. The HTC values where the integrated cooling becomes better than the AlSiC, and copper baseplates are shown with dotted red lines.

As shown by Figure 49 and Figure 50 when comparing the two baseplate models the solid copper baseplate always has a lower maximum temperature than the AlSiC baseplate, by an average of 5.2°C. The DBC integrated cooling model however had two transition points where the performance increased above the AlSiC, and then the copper baseplate. At 35 and 70 $\text{kW/m}^2\text{-K}$, the maximum temperature of the integrated cooling model dropped below the temperature of the AlSiC, and copper baseplates respectively. This was true for all applied heat loads and for both 50 and 100°C ambient fluid

temperatures. These HTC values were significantly larger than the largest evaporative HTC value found experimentally. This implies that for these heat fluxes evaporation may not be a suitable candidate for cooling, however boiling falls within the range of $80 \text{ kW/m}^2\text{-K}$. Although this study did not reach sufficient heat transfer coefficients similar studies with sintered copper particles have. A study performed with sintered copper wicks was able to achieve a substrate temperature of $\sim 105^\circ\text{C}$ at 100 W/cm^2 [92], where the largest heat flux of this model was only 101 W/cm^2 with a substrate temperature of 120°C . Other studies have also shown spray cooling directly on DBC to be able to achieve heat transfer coefficients as high as $280 \text{ kW/m}^2\text{-K}$ [93], making the direct cooling a viable option.

2.5.7 *Summary and Conclusions*

After experimentally measuring both the effect of a sintered copper particle wick thickness, and width on the heat transfer performance the system was compared to models to understand the possible mechanism of dry out. Changing the wick thickness from 1.138 to 0.603 mm did not have a significant effect on the thermal resistance of the samples, however it did play a significant role in the dry out heat load. By applying a capillary pressure model it could be shown that the dry out was due to the inability of the wick to provide enough fluid to the heated surface, and increasing the wick thickness aided in the water resupply. Similarly increasing the width of the samples did not significantly reduce the thermal resistance, but it also played a role in the dry out power limit. Although using a simplified capillary pressure model did not explain the dry out so a critical surface super heat for boiling model was compared. It was shown that the particles the wick was made of were within the range to make pore sizes which could induce boiling at the temperatures

where dry out was experimentally measured. Therefore it was determined that for the large area wicks the capillary pressure was not the limiting factor, but the boiling limit was. Increasing the size from 17 by 15 mm to 20 by 25 mm significantly reduced the thermal resistance at very low power levels, however above ~30 W the thermal resistance was only reduced by about 0.5 K/W. Then further increasing the width to 50, and 75 mm did not reduce thermal resistance significantly, although it did increase the heat load before dry out.

In order to evaluate the possible benefits of an integrated cooling method such as this, an IGBT module was numerically modeled and modified to compare. Three comparison were made, a module with an AlSiC baseplate, another with a copper baseplate, and the integrated model with no base plate. This numerical model showed that the integrated cooling method was able to reduce the maximum temperature in the module lower than either the AlSiC, or copper baseplates with high enough HTC values. This study was therefore able to show that integrating a copper wick onto a DBC substrate would be able to improve performance while also reducing the size and weight of power module. Another potential method for reducing the thermal resistance between the chip and the cooling solution is to bond the AlN dielectric layer directly to the baseplate. This reduces the number of contact resistances between the cooling solution and the junction. In Chapter 3 a novel bonding method is introduced to attach the AlN directly to an AlSiC baseplate at lower processing temperatures than DBC.

CHAPTER 3. COMPOSITE BONDING METHOD FOR JOINING ALUMINUM NITRIDE TO ALUMINUM SILICON CARBIDE

3.1 Introduction

In order to reduce the operating temperature and improve the reliability of power electronic substrates it is important to reduce the thermal resistance between the chip and the cooling solution. In this chapter, a method for bonding AlN to an AlSiC baseplate through the use of a composite Al-Cu-SiC eutectic bond is described, and the bond is analyzed. The back ground and methodology with the composition, and heating profile will be detailed and discussed. The bond was imaged with scanning electron microscopy to determine the thickness, and qualitatively evaluate the bond. The chemical composition was then analyzed with energy-dispersive X-ray spectroscopy to determine the composition through the bond layers. The electrical and mechanical reliability was evaluated with several experiments. The thermal conductivity, hardness and elastic modulus were also measured and compared to similar bond materials. The bond properties were used in numerical modeling to display the advantages to directly bonding the AlSiC baseplate to the AlN in a typical IGBT circuit.

3.2 Sample Fabrication

3.2.1 Bonding Process Background

The AlN ceramic was attached to the AlSiC baseplate with a transient liquid phase bonding (TLP) process using an Al/Cu eutectic described by MacDonald *et al.* [94]. This process entails putting two different metals in contact in a specific bulk ratio, and heating

them above the eutectic melt temperature, but below the melting temperature of either individual metal. Initially during the heating process both metals remain solid as they diffuse into each other, however eventually the composition will reach the liquid regime as shown in Figure 51 for Cu/Al.

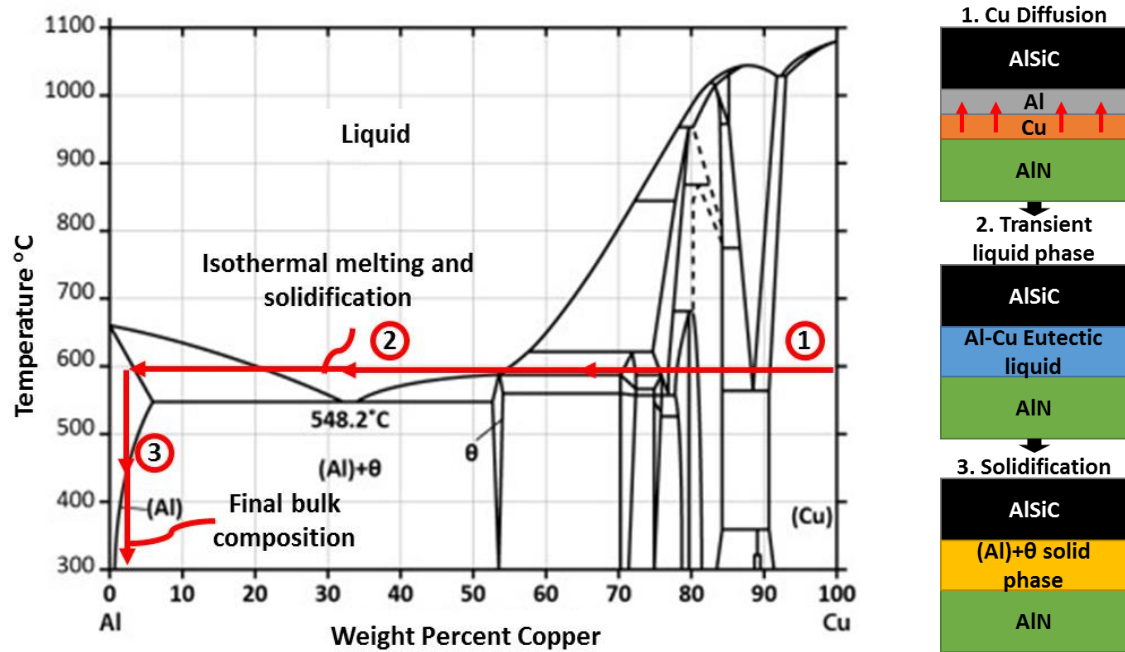


Figure 51. Binary phase diagram and bonding process for copper and aluminum, showing the diffusion and changing composition of the bond layer as Al diffuses into Cu during the heating process.

As the metals continue to dissolve into the liquid, the composition eventually passes into the liquid/solid regime and partially solidifies. Then as copper diffuses into the solid the system eventually begins to solidify again. The system is then left to naturally cool and the metals diffuse into each other to reach their steady state composition. In this case the final composition was a mixture of Al, Cu and θ phase, (Al_2Cu). A similar process was performed by Kuromitsu *et al.* [95] where Cu was deposited with electron beam deposition

for a final bulk composition of 0.02% Cu, however due to the low Cu content, no θ phase was present in the final bond.

The bonds in this chapter were made by stacking two 50 μm thick Al foils and one 12.5 μm Cu foil in between an AlN ceramic and an AlSiC baseplate as shown in Figure 52. The AlSiC also had a layer of Al 356 alloy on top (~ 65 μm thick), which was 6.5 – 7.5 wt.% Si. The composition of the bond based on the two Al foil layers, the Cu layer and the Al 356 layer was 77.9 wt.% Al, 20.2 wt.% Cu, and 1.9 wt.% Si. The stack sequence was chosen such that the point contacting the AlN would initially be pure copper, and the composition would change according to the arrow shown in Figure 51. Therefore, placing the Cu in contact with the AlN forced the layer directly next to the AlN to pass fully through the liquid regime. If a layer of aluminum was held in contact with the AlN, then there is no way to ensure that some of the Al foil did not remain solid through the entire process, leaving un-bonded areas.

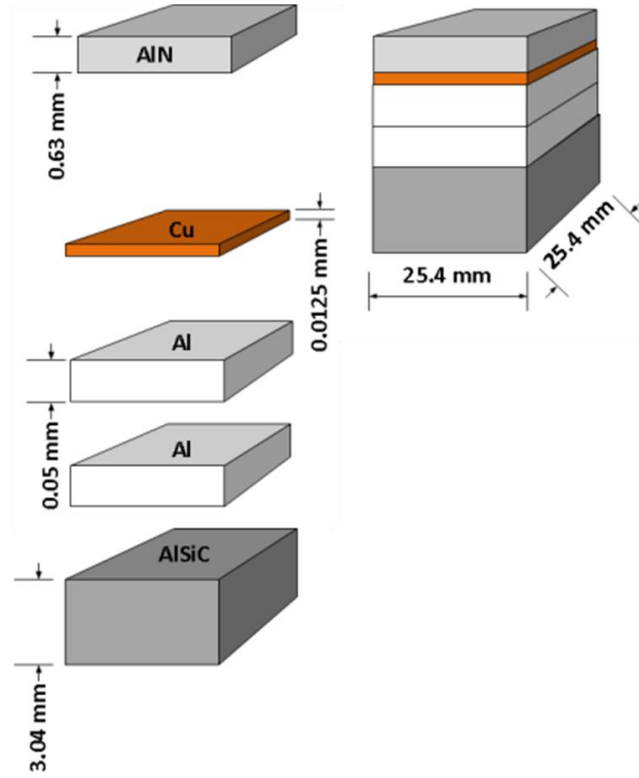


Figure 52. Bonding stack showing the stack sequence and size of the AlN, Cu, Al, and AlSiC layers.

The solid-state diffusion of species in this study was governed by Fick's second law of diffusion which predicted how the concentration would change with time, and is given in the 1D form by equation 3.1:

$$\frac{d\Phi}{dt} = C_d \frac{d^2\Phi}{dx^2} \quad 3.1$$

where Φ is the concentration, C_d is the diffusion constant, t is time, and x is the spatial dimension. The diffusion constant is dependent on the two diffusing materials, and is a function of time given by equation 3.2:

$$C_d = C_o e^{\frac{-Q_d}{RT}} \quad 3.2$$

where C_o is a material constant, ($6.5\text{E-}5 \text{ m}^2/\text{s}$ for the Al-Cu systems), Q_d is the activation energy for diffusion, (136 kJ/mol for the Al-Cu system), R is the molar gas constant, and T is the temperature, [96]. As C_d exponentially increases with T , it is clear that at higher temperatures diffusion speed will increase rapidly. By modeling the Al-Cu system with these equations, an estimate for the required diffusion time before melting occurred was determined for the specific system in the next section.

3.2.2 Bonding Process

In order to ensure there were no contaminants within the bond each component was first cleaned with a 25% HCl solution at room temperature, before being rinsed with DI water, and isopropanol. The HCl solution helped to remove aluminum oxide which may have formed on the Al foils, and AlN while not affecting the AlN, [97]. After cleaning of each piece, the stack was placed in a graphite bonding rig as shown in Figure 53 below. Graphite was used as it is a refractory material often used to make crucibles, and as a mold for molten metals.

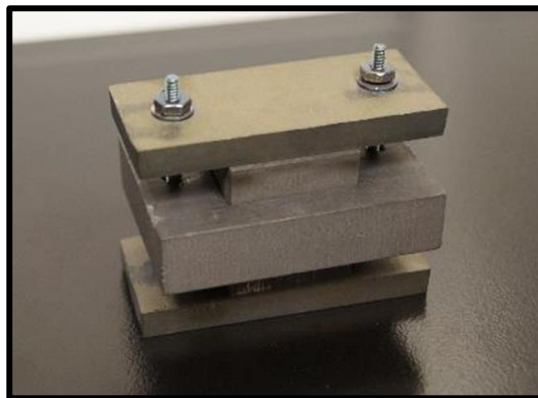


Figure 53. Bonding rig showing the graphite and stainless steel clamp.

The stainless steel clamp was hand tightened to hold the sample in place, and keep the foil layers flat without applying additional pressure to the bond. The rig was then placed in a tube furnace, which was sealed and held under vacuum to a pressure of ~ 20 mTorr. The vacuum was used to avoid the formation of oxides within the bond layer. The temperature was increased to 530°C and held for 20 minutes then increased to 565°C and held for 30 more minutes before turning off the power and allowing it to cool naturally to ambient as shown in Figure 54.

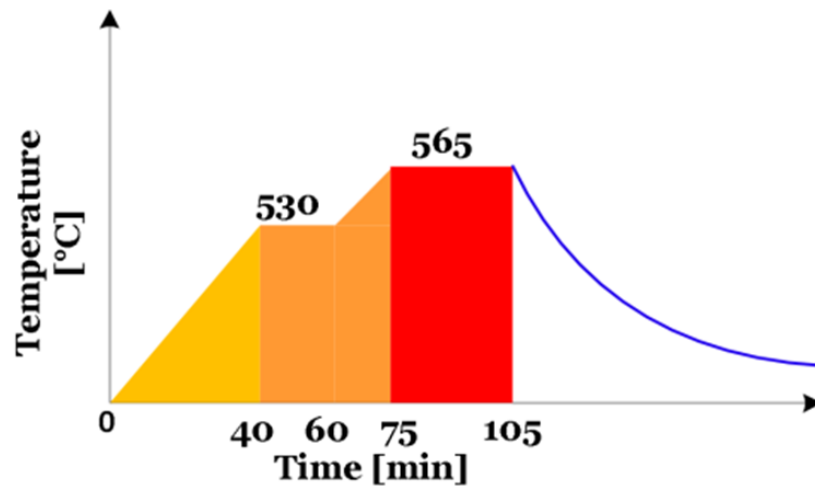


Figure 54. Temperature profile followed by the furnace showing the ramp time, hold time, and natural cooling after a total of 105 minutes.

The 20 minute hold time at 530°C was used to allow the Cu to diffuse into the Al before reaching the melt temperature. This way when the melt temperature was finally reached the bond would melt more homogenously as opposed to melting at a small interface layer first, and the liquid layer slowly growing. The hold time of this step was determine by solving equations 3.1, and 3.2 with finite differencing using third order approximations for the derivatives. For the models a time step of 0.001 s, and a spatial step

size of 0.1 μm where applied, with the diffusion coefficient recomputed for each temperature.

Although an exact solution exists for 1D diffusion, a numerical model was chosen as the temperature changes with time, so the diffusion constant C_d was not constant at all times. The temperature was decided to be 530°C to avoid possible overshoot into the liquid regime before diffusion was complete, while also being high enough to allow for rapid diffusion. Applying this temperature profile to the numerical model resulted in a final composition profile through the Cu foil and two Al foils as shown in Figure 55 below. According to this model at the time when the temperature reaches 565°C approximately 45 μm of the bond thickness will turn to mostly liquid.

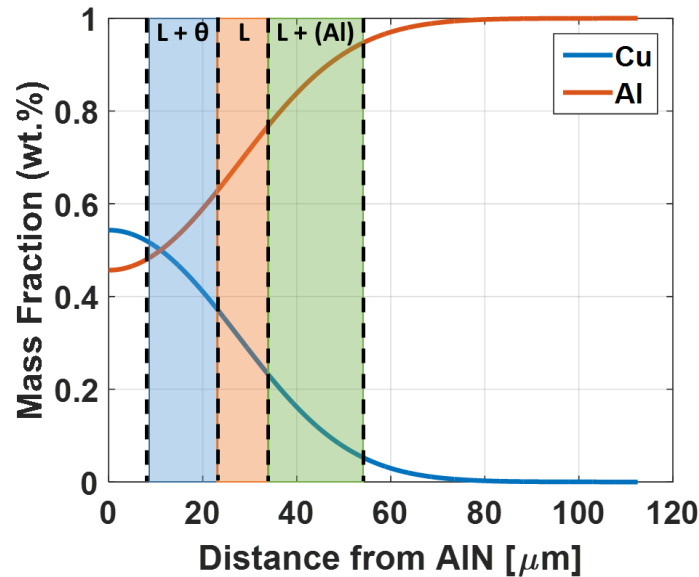


Figure 55. Composition of the Al-Cu foils as a function of distance from the AlN layer at the time when the temperature reaches 565°C. This shows the regime which is purely liquid, the liquid + θ regime, and the liquid + Al regime.

This pre-diffusion step provided one main advantages over simply increasing to the melt temperature immediately. First, by increasing the amount of liquid which formed at

one time, the effect of leakage was reduced. The early liquid composition had a high Cu content, so if a thin interface layer leaked it would take a disproportionately large amount of Cu with it.

After being heated in the furnace the sample was removed from the vacuum when it reached ambient temperature. In order to prepare it for SEM imaging the sample edges were polished with SiC grinding paper with 46 to 4 μm particle sizes, and then an alumina solution with 1 to 0.05 μm particles. The sample was then cleaned with sonication for 30 minutes to remove excess particles due to polishing.

3.3 SEM and EDS analysis

Scanning electron microscopy (SEM), was used to image the bond between the AlN and the AlSiC, while energy-dispersive X-ray spectroscopy (EDS) was used to determine the bond composition. Imaging the bond with SEM was an important step to visually evaluate the consistency of the bond, and to track movement of the SiC particles as shown in Figure 56. The EDS analysis was essential to quantify the actual bond composition and also to track diffusion of specific species through the layers with a linescan.

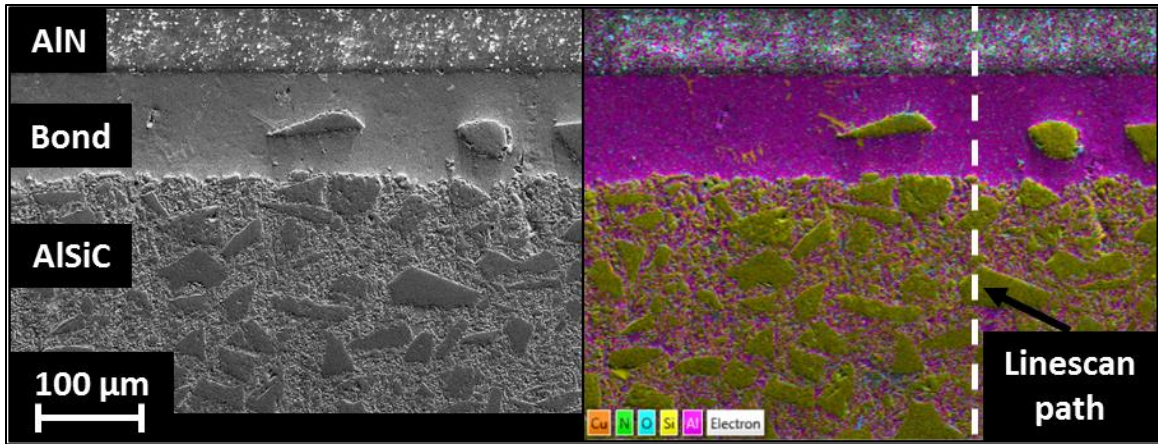


Figure 56. SEM (Left), and EDS (Right) images showing the AlN on top with the bond, and SiC particles, some of which have drifted into the bond line. The EDS image also indicates the path followed for the linescan analysis with a dotted line.

Due to the inclusion of the SiC particles from the AlSiC, some of these particles migrated into the bond as shown in Figure 56. By evaluating SEM images at several locations across the bond it was found that the average bond thickness was 100 μm , but could range anywhere from 90 to 180 μm . This range was mainly due to bond material leakage and the large range in the SiC matrix evenness across the surface. Using the EDS image the composition of the bond area was found to be 93.0 wt.% Al, 0.6 wt.% C, 1.5 wt.% Cu, 0.3 wt.% N, 1.7 wt.% O, and 2.8 wt.% Si. The oxygen in the bond was likely due to surface oxidation of the Al, and the nitrogen and carbon were trace amounts left from the grinding process. Using the binary phase diagram in Figure 51 with 1.5 wt.% Cu, the ratio of the θ phase was estimated to be 2.8 wt.%, with Al + Cu + Si being 97.2 wt.%. This differed significantly from the estimation based only on the materials in the top layers, (77.9 wt.% Al, 20.2 wt.% Cu, and 1.9 wt.% Si). This was due to the exclusion of the Al 356 in the SiC matrix, which accounts for 37 vol.% of the bulk 3 mm thick AlSiC. Including this volume of Al the estimation becomes 92.9 wt.% Al, 1.3 wt.% Cu, and 5.8 wt.% Si.

This was much more similar to the mass fractions measured with EDS, implying that melting may have occurred more deeply within the AlSiC matrix. Since the backside of the AlSiC did not appear changed after bonding, it was assumed that after the area near the surface melted, the Cu continued to diffuse through the AlSiC until the steady state composition was reached.

In order to track the diffusion of different species through the length of the bond EDS was used to scan a line path down the width of the sample as shown in Figure 56 above. This measurement was performed at several different locations, but only one representative location is shown below in Figure 57, as all scans had comparable results.

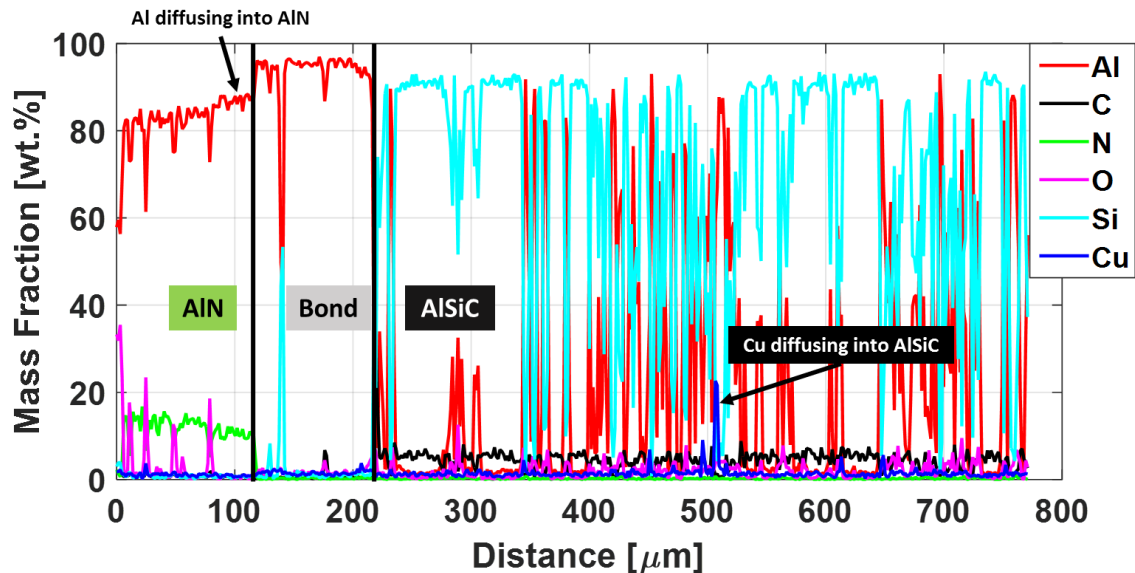


Figure 57. EDS linescan results showing the three distinct regions of AlN, the bond, and the AlSiC. This plot also shows the diffusion of Cu as far as 300 μm into the AlSiC, and the diffusion of Al into the AlN as indicated in the plot.

The SiC particles are indicated in Figure 57 by the spikes in Si within the AlSiC layer, which is known because of the simultaneous spikes in carbon. However, the Si spike in the bond region was not accompanied by a spike in carbon, indicating this was a Si precipitate

present because of the Si in the Al 356 alloy. The diffusion of Al metal into an AlN crystal structure was not expected as the 1:1 molar ratio should remain constant, therefore this was investigated by analysis of AlN alone. To determine if the Al metal was present beforehand EDS analysis was performed on a lone sample of AlN as shown in Figure 58 below.

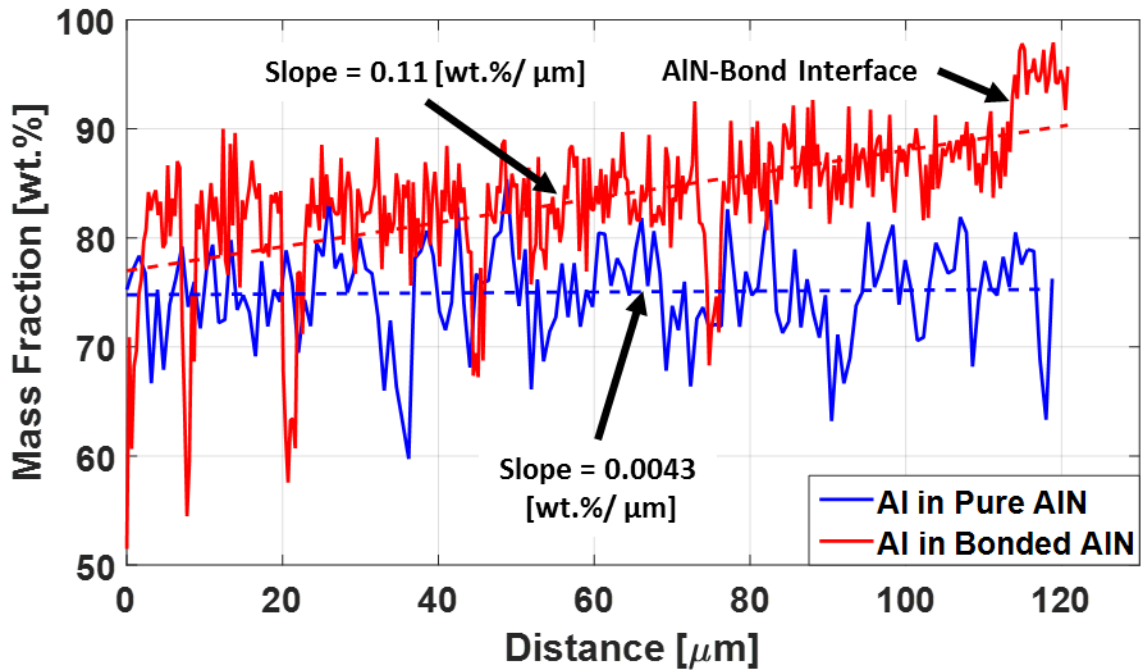


Figure 58. Plot of mass fraction of Al through the AlN substrate for both an un-bonded, and bonded AlN showing the slope of the line computed with linear regression.

The Al concentration within the un-bonded AlN sample can be seen in Figure 58 to be constant through the AlN. However, the bonded AlN sample clearly shows an increase in the Al concentration closer to the AlN-Bond interface with a slope 25 times larger than the un-bonded sample. This shows that the Al leaked as far as 120 μm into the AlN substrate. This occurred because AlN substrates are manufactured by sintering AlN particles together using a yttria (Y_2O_3) additive to reduce the processing temperature and aid in densification [98]. Therefore, there were grain boundaries and voids within the AlN

which the Al melt was able to fill. Although this is advantageous for the bond strength by improving adhesion, Al metal leaking deep into the AlN could affect the dielectric properties. Therefore, this was investigated in the next section, Properties of Bond Material, to determine if the dielectric strength was reduced.

3.4 Properties of Bond Material

3.4.1 Dielectric Strength

Power electronics devices often must operate on the order of tens of thousands of volts, so it was important to verify that the dielectric strength of the AlN was not affected by the bonding process. The dielectric strength of a material is the ability of the material to remain insulating with voltage applied, and is defined as the maximum blocking voltage per length of material. In order test the dielectric strength two copper electrodes were attached to either side of the bonded sample with copper tape as shown in Figure 59 below.

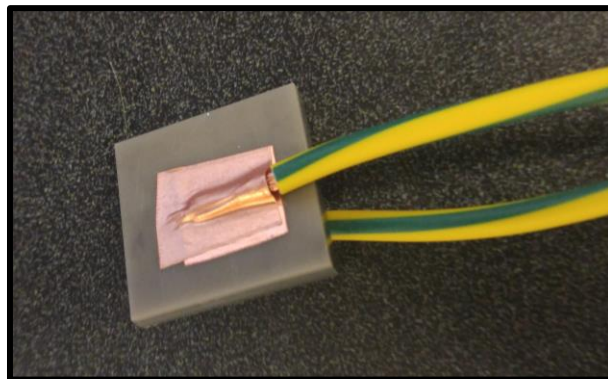


Figure 59. Bonded sample, (25.4 by 25.4 mm), with 1.016 mm thick AlN layer, and two copper electrodes attached by conductive copper tape.

A voltage was then applied to the sample and increased until current began to flow through the AlN. Since the dielectric breakdown of air was much less than the AlN, the sample had

to be submerged in Fluorinert (FC-72) from 3M, (a dielectric fluid with a strength of 15 kV/mm). As the electrodes were placed ~5 mm from the edges of the sample, the FC-72 had a total blocking voltage of ~75 kV. While submerged in FC-72 the AlN began to conduct electricity at 18 kV, leading to a dielectric strength of 17.7 kV/mm. The test was then repeated with an un-bonded sample of AlN, and again dielectric breakdown occurred at 18 kV. This was also consistent with the AlN manufacturers estimated value of 17 kV/mm for the dielectric strength [99]. This confirmed that neither the bonding process nor the leakage of Al into the AlN grains reduced the dielectric strength of the AlN.

3.4.2 *Young's Modulus and Hardness*

It is important to understand the mechanical behaviour of the bond material so that it can be modelled under thermal stresses. Therefore the hardness and the Young's modulus were both measured with a diamond tipped nanoindenter, (Hysitron Ti 900 Triboindenter), calibrated with fused silica. The calibration was performed over a range of 0 to 600 nm indentation distance, encompassing the full range of 0 to 500 nm which the bond material displaced. In order to test the properties of the bond material alone, a new sample was made of the AlSiC layer with the Al and Cu foil on top, but without the AlN layer. This way the equivalent material composition was produced, but there was a larger area to access the bond material. After sample fabrication the topside of the bond material was polished with the same procedure used to prepare the sample for SEM imaging.

3.4.2.1 Operating Theory of Nanoindentation

A standard nanoindentation test uses a diamond tip with known Young's modulus and Poisson's ratio to deform a material with unknown properties. When force is applied

to the tip, it deforms the sample surface while measuring the applied force and the deformation distance. Then it continues to measure the force as it unloads out of the material. In order to accurately determine material properties a calibration for both the tip area function and machine compliance are both required. The hardness, Ha , is measured by the maximum load applied P_{max} , and the residual indentation area, A_r , computed from the tip displacement calibration as shown in equation 3.3.

$$Ha = \frac{P_{max}}{A_r} \quad 3.3$$

The reduced Young's modulus is computed from the slope of the unloading curve where the deformation is purely elastic as shown by equation 3.4:

$$E_r = \left(\frac{dP}{dh} \right) \frac{\sqrt{\pi}}{2\sqrt{A_h}} \quad 3.4$$

where h is the tip height, and A_h is the indented area at that tip height. The actual Young's modulus can then be computed from E_r using the known properties of the diamond indentation tip. A typical loading curve is shown below in Figure 60 to show the portions of the curve used to compute the Young's modulus, and hardness.

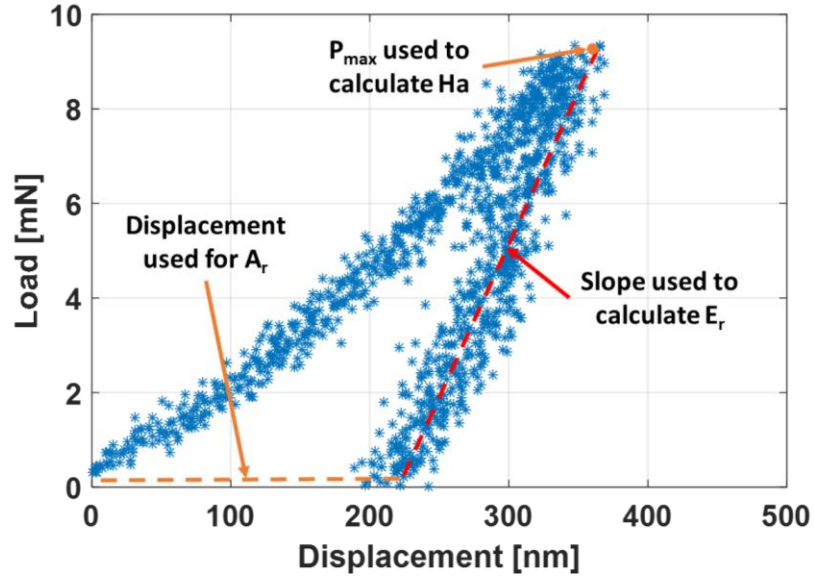


Figure 60. Example loading and unloading curve used to measure the Young's Modulus, and the hardness of the bonded material.

3.4.2.2 Young's Modulus and Hardness Measurements

Once the calibration was complete the bond material was indented to extract the Young's modulus and hardness values. To perform the test the nanoindenter made 9 indentations per run in a 90 by 90 μm grid array as shown in Figure 61 below.

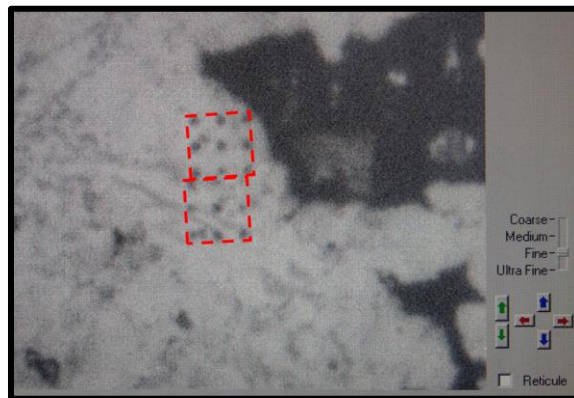


Figure 61. Indentation grids created by the nanoindenter shown within the 90 by 90 μm red squares, (30 μm spacing between each point.)

For each indentation a loading/unloading curve was generated, however the software was not able to extract a value of Young's modulus for every indentation. Out of the 18 total points, 15 values for Young's modulus and hardness were extracted. These values for Young's modulus and hardness were plotted below against the plastic displacement in Figure 62 and Figure 63 respectively.

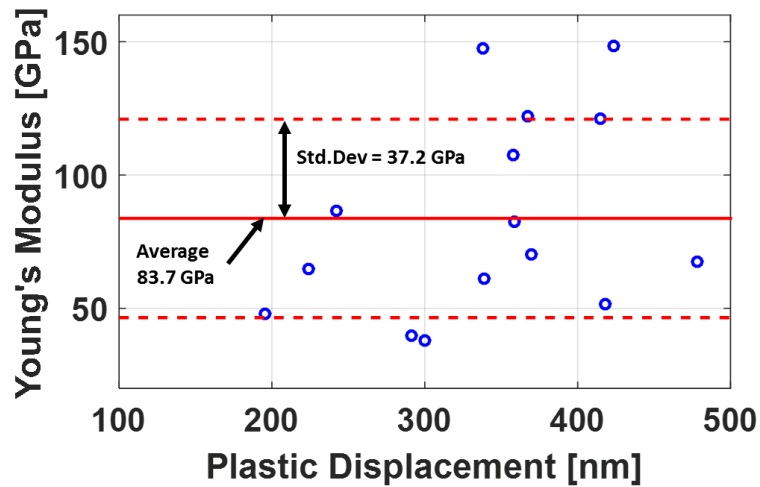


Figure 62. Plot of Young's Modulus showing the average of 83.7 GPa with a solid red line, and the standard deviation of 37.2 GPa with dotted red lines.

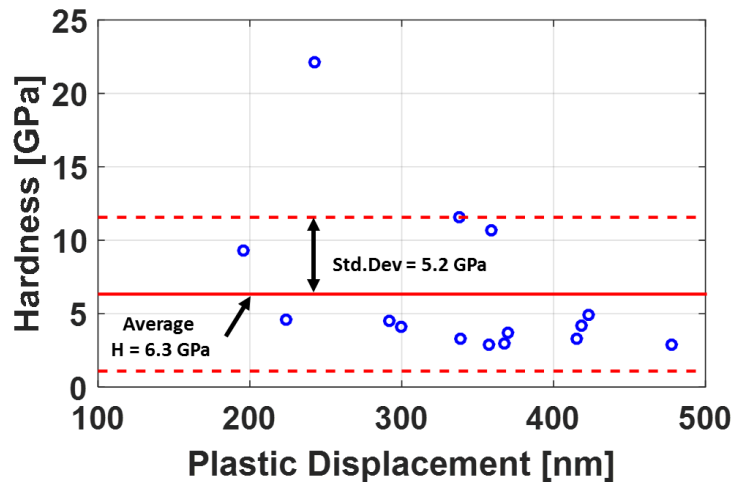


Figure 63. Plot of Hardness showing the average of 6.3 GPa with a solid red line, and the standard deviation of 5.2 GPa with dotted red lines.

When compared to pure Al which has a Young's modulus of 75 GPa the bond material was slightly more rigid. This was possibly due to the bond being a mixture of Al and the θ phase, (Al_2Cu), which has modulus of 120 GPa [100]. Another cause could have been the SiC particles near the surface which have a modulus of 410 GPa, and could have aided in resistance to elastic deformation. The large standard deviation in data was also attributed to the SiC particles which, (on the length scale of 90 μm), were not uniformly distributed beneath the surface.

The hardness of the bond was measured to be 6.3 GPa, significantly larger than the hardness of Al, which was 0.5 GPa. However the value was also much smaller than the hardness of SiC, being 28 GPa. The increase in hardness could be due to precipitate hardening which introduces precipitates, (the 2.8 wt.% θ phase), into the matrix to obstruct the movement of dislocations [47]. Since the hardness is a measure of the materials resistance to permanent plastic deformation, this increase implies the bond will be much more resistant to deformation than a pure Al bond. The hardness also had a large standard deviation which could have been due to the SiC particles spread non-uniformly beneath the surface.

3.4.3 Thermal Conductivity

Another important thermo-physical property of the bond was the thermal conductivity as this dominates the thermal transport abilities of the material. This was measured with a laser flash diffusivity technique. Laser flash diffusivity is a transient heat flow measurement where one side of a sample absorbs a short laser pulse, while the temperature change on the other side is monitored. This temperature change as a function

of time can then be fit to numerical or analytical models to compute the thermal diffusivity of the material.

3.4.3.1 Operating Theory of Flash Diffusivity

The thermal diffusivity is a measure of how fast a temperature disturbance can move through a material, and is related to thermal conductivity by equation 3.5:

$$\alpha = \frac{k}{\rho C_p} \quad 3.5$$

where α is the thermal diffusivity, k is the thermal conductivity, ρ is the density, and C_p is the specific heat capacity. The laser flash method involves heating one side of a material with a laser pulse, and then monitoring the transient temperature of the other side via an IR signal as shown in Figure 64.

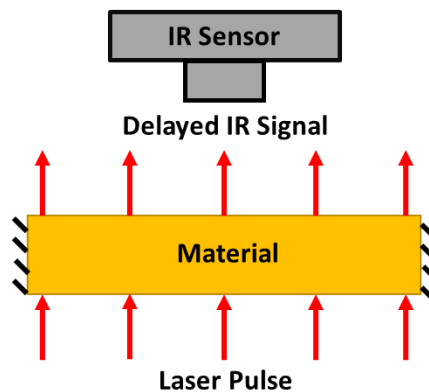


Figure 64. Laser flash diffusivity diagram showing the material with the laser pulse on the bottom, and the resulting delayed IR signal with an IR sensor on top.

Other methods for measuring thermal conductivity typically require thermocouples and applied heat loads, which introduces error due to contact resistances. This method only requires contacts at the edges to hold the sample, reducing uncertainty in the measurement.

The transient temperature profile read from the IR sensor is then fit to a theoretical model to determine the thermal diffusivity of the material. In the 1D adiabatic case for a single layer material the model by Parker *et al.* [101] can be applied. This model is defined by two dimensionless parameters V , and ω , the dimensionless temperature rise, and a modified Fourier number, described by equations 3.6, and 3.7 respectively:

$$V(t) = \frac{T_s(t)}{T_{\max}} = 1 + 2 \sum_{n=1}^{\infty} (-1)^n e^{-n^2 \omega} \quad 3.6$$

$$\omega(t) = \frac{\pi^2 \alpha t}{L^2} \quad 3.7$$

where $T_s(t)$ is the temperature of the top surface, T_{\max} is the maximum temperature of that surface, L is the thickness of the material, and t is time. By plotting the V vs. ω curve shown in Figure 65, two relationships can be seen to determine α .

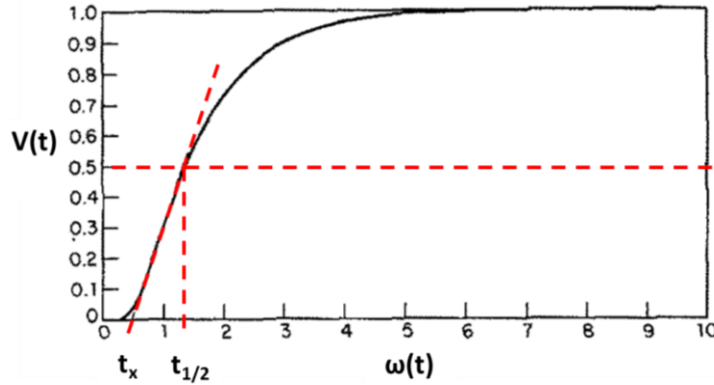


Figure 65. Plot of dimensionless temperature rise vs. a modified Fourier number, showing the lines used to calculate t_x and $t_{1/2}$ for determining thermal diffusivity [101].

One of these relationships is that when V is equal to 0.5, then ω is equal to 1.38, allowing α to be computed from equation 3.8:

$$\alpha = \frac{1.38L^2}{\pi^2 t_{1/2}} \quad 3.8$$

where $t_{1/2}$ is the half rise time, the time it takes the sample temperature to reach half of the maximum temperature. The second relationship is that by extrapolating the linear portion of the curve to the x-axis, the value of ω will equal 0.48, giving equation 3.9.

$$\alpha = \frac{0.48L^2}{\pi^2 t_x} \quad 3.9$$

Where t_x is the time axis intercept of the temperature vs. time curve. The thermal conductivity of the material can then be calculated from equation 3.5 above. For a multilayer material where the properties of the other layers are known, a model described by Lee *et al.* [102] is applied to determine the thermal diffusivity of the unknown material. This analytical model applies similar principals as the single layer model, however it is described by relative material properties, and is too extensive to enumerate here.

3.4.3.2 Thermal Conductivity Measurements

In order to determine the thermal diffusivity of the bond material, the thermal diffusivity of both the AlN and AlSiC were first measured with the laser flash method using the Hyperflash system. In order to ensure energy absorption from the laser, and irradiation to the sensor both sides of all sample were coated with a thin graphite spray coating to increase the emissivity of the surface. The sample holder was also made of insulating ABS plastic to reduce the heat loss at the edges. The experiment took place in a vacuum sealed chamber held at 25°C to eliminate variation from ambient temperature changes. For the single layer materials the software computed the thermal diffusivity with a model by

Cowen [103], similar to the aforementioned 1D model but modified to account for heat losses. The bonded sample was then measured the same way, and using the thermal diffusivity computed for the AlN, and AlSiC the thermal diffusivity of the bond layer was determined. The flash was repeated three times and an average thermal diffusivity was reported. The material thermal diffusivity, density, heat capacity, and thermal conductivity are all reported in Table 7 below. The density of the bond was computed as the weighted average between the density of Al, 2700 kg/m³, and the density of Al₂Cu, 4400 kg/m³, using the estimated ratio of 97.2 wt.% Al, and 2.8 wt.% Al₂Cu, estimated from the EDS analysis earlier.

Table 7. Material properties of the substrate materials.

Material	Thermal Diffusivity (m²/s)	Density (kg/m³)	Specific Heat (J/kg-K)	Thermal Conductivity (W/m-K)
AlSiC	7.94e-5 ± 2.1e-7	2870	741	168.8 ± 0.5
AlN	6.47e-5 ± 2.1e-7	3260	740	156.1 ± 0.5
Bond	5.17 e-5 ± 2.3e-6	2750	853, [104]	121.2 ± 5.3

The thermal conductivity computed here was lower than the thermal conductivity measured in literature, 174.1 W/m-K, for a similar Al-Cu composition [104]. This was possibly due to the addition of SiC, or Si particles in the bond which have a lower thermal conductivity than the bulk bond material. This thermal diffusivity measurement also includes the contact resistance of the bond. This extra resistance reduces the effective thermal conductivity, even if the thermal conductivity of the bond material was higher. The thermal contact resistance of the bond was estimated with equation 3.10, assuming the bond material had a thermal conductivity of 174.1 W/m-K, and a constant thickness of 146 µm:

$$R'' = L \left(\frac{1}{k_e} - \frac{1}{k_b} \right) \quad 3.10$$

where L was the bond thickness, k_e was the effective thermal conductivity, and k_b was the theoretical bond thermal conductivity. This resulted in an estimated bond contact resistance of 0.37 K-m²/MW. This means that by reducing the bond layer thickness the overall thermal contact resistance could be reduced from 1.2 a minimum of 0.37 K-m²/MW.

3.5 Fatigue and Thermal Stress

In order to estimate the bond life time accelerated life testing was used, which allows the lifetime at a smaller temperature cycle to be estimated by the lifetime at a large temperature cycle. The acceleration factor can be computed from the Coffin-Manson equation [105] shown below by equation 3.11:

$$N_{fa} = N_{ft} \left(\frac{\Delta T_{test}}{\Delta T_{use}} \right)^m \quad 3.11$$

where N_{fa} is the actual number of cycles to failure, N_{ft} is the number of cycles until the test sample failed, ΔT_{test} is the temperature change at which testing is done, ΔT_{use} is the expected temperature change for normal use, and m is the Coffin-Manson exponent. For a typical commercial power electronic device the temperature use range will 70°C, and for aluminum m is ~2 [37]. Testing was performed with a Tenney environmental chamber to cycle the temperature. The temperature of the chamber was cycled between -60°C, and 200°C with a heating rate of 2°C/min, and a cooling rate of 3°C/min. Three samples were tested, and after 20, and 100 cycles they were removed from the chamber and visually

inspected to determine if they had delaminated. None of the samples showed any signs of delamination or cracking after 100 cycles. By applying equation 3.11 the bond life was estimated to be at least 1380 cycles with a 70°C temperature change. This was significant improvement upon DBC which will typically show delamination and cracking around 40 cycles in similar testing conditions [106, 107].

3.5.1 Finite Element Stress Modelling

To better evaluate the stresses which cause cracks and delamination in the AlN and bond material finite element modeling was performed using ANSYS. In this study a representative IGBT module was designed, based on the ABB HiPak module with 6 integrated IGBTs [91], similar to the IGBT model used in Chapter 2. In order to reduce computational time of the model the system was reduced to a single unit cell of the HiPak module as shown below in Figure 66. A static structural model was built with a constant temperature condition applied to all module components, and the resultant principal stresses were found. To compare the novel bonding method, (AlN/AlSiC), to a typical DBC package two models were made. One model utilized a typical DBC stack with IGBTs on top of the DBC, and DBC attached to the AlSiC with a layer of Au-Sn solder. The second model applied the novel bonding method and replaced the Cu and the solder with a layer of the bond material, as shown in Figure 67. The material parameters and thicknesses of each layer are summarized in Table 8 below.

In order to properly account for residual stresses resulting from the manufacturing processes the stress free temperature (reference temperature) was modelled differently for each material. In the standard DBC model the copper and AlN reference temperature was

set to 1000°C, as this is the temperature at which the Cu/O eutectic bond solidifies [108]. In the AlN/AlSiC model the reference temperature was set to 600°C, the solidification temperature of the Al/Cu eutectic. The stress free temperature of the solder, silicon devices, and AlSiC (in the DBC model) was set to 280°C since this is the temperature at which the device, and AlSiC would be attached by the Au-Sn solder. The bond material was modelled with the CTE of both Al and AlSiC as upper and lower bounds respectively. Since it is known that SiC particles migrate into the bond, the CTE must lie between the CTE of Al and AlSiC. The inner portion of the bolt holes were modelled as fixed support boundaries since this is where the IGBT would be held still by the mounts.

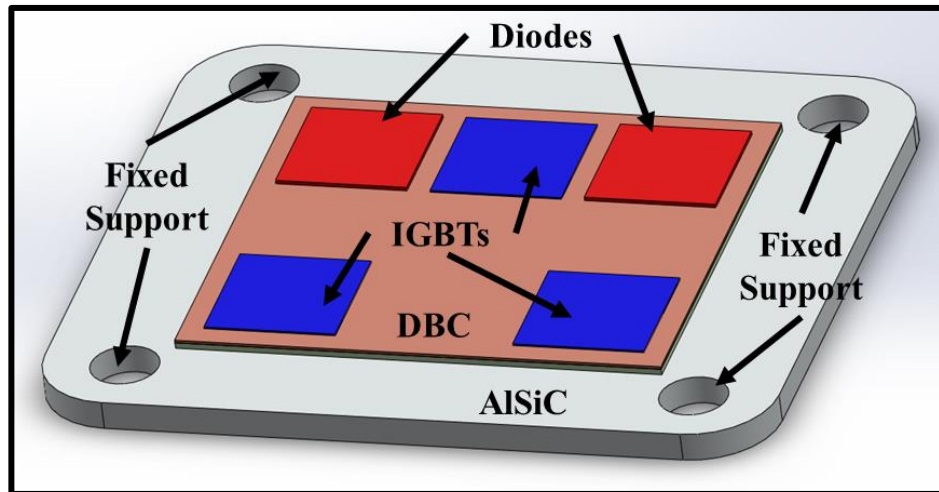


Figure 66. Single unit cell of ABB HiPak IGBT inverter module showing the IGBTs in blue, with the diodes in red, with the DBC attached to the AlSiC baseplate.

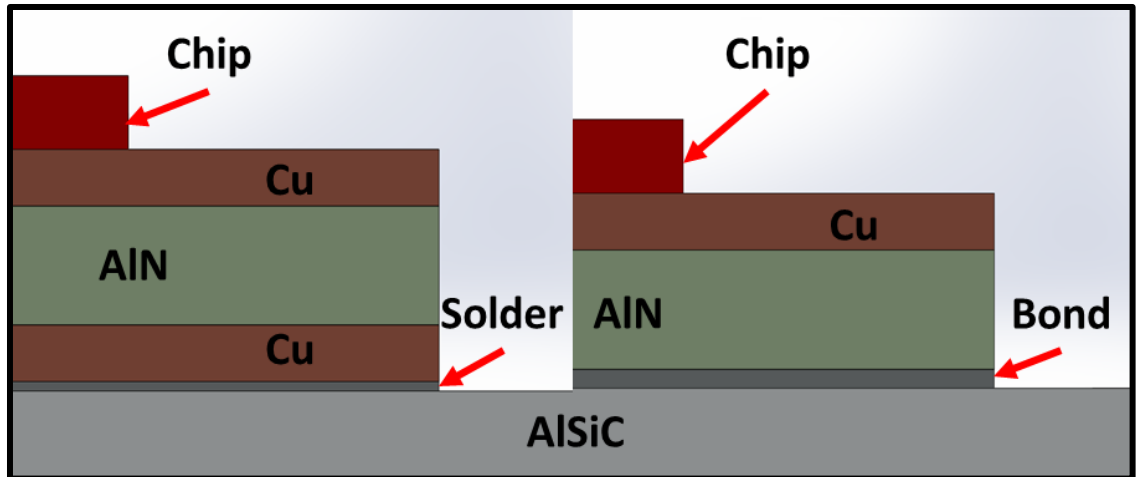


Figure 67. ABB HiPak IGBT stack showing the location of the DBC, and solder (Left), compared to replacing the Cu and solder layers with the bond (Right).

Table 8. Material Parameters applied to the finite element model.

Material	CTE ($10^{-6}/^{\circ}\text{C}$)	Young's Modulus (GPa)	Thickness (μm)	Reference Temperature ($^{\circ}\text{C}$)
Silicon	2.8	131	190 (IGBT) 390 (Diode)	280
Au-Sn Solder	16	59	50	280
Copper	18	110	300	1000 (DBC) 600 (Bond)
AlN	4.5	330	630	1000 (DBC) 600 (Bond)
AlSiC	8	188	3000	280 (DBC) 600 (Bond)
AlN/AlSiC bond	22.3, 8	83.7	100	600

In this model there are two important areas of interest where failure often occurs, the AlN layer and the bond/solder layer. Therefore the principal stresses in each of these layers was averaged over the body and plotted below as a function of temperature in Figure 70 and Figure 71. The average value was reported because the stress was seen to not change appreciably through the bulk of each material. In order to ensure the model was independent of mesh size the mesh was refined until the maximum principal stress in the

AlN and bond material changed by less than 2%. The results of the mesh independence study are shown in Figure 68 for the standard DBC/solder model and Figure 69 for the novel bonding method.

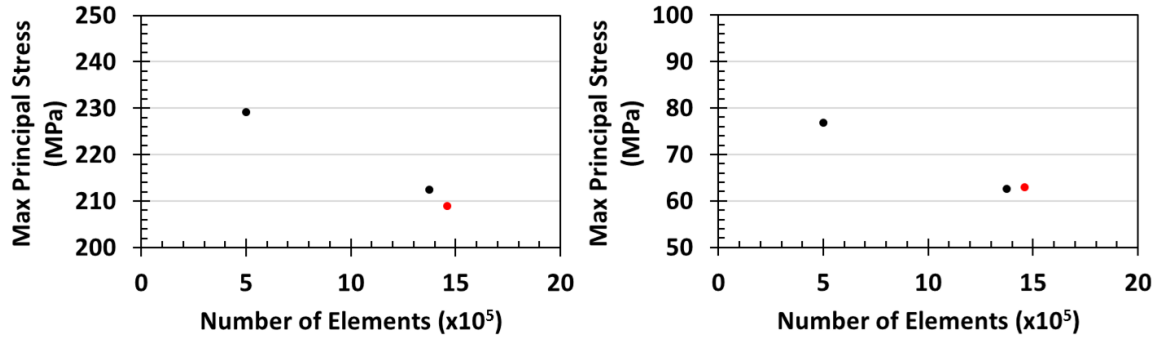


Figure 68. Change in maximum principal stress of the standard DBC model as the number of elements in the mesh was increased, showing the stress in the AlN (Left), and the stress in the solder (Right). The mesh size used for further modeling was indicated by the red marker.

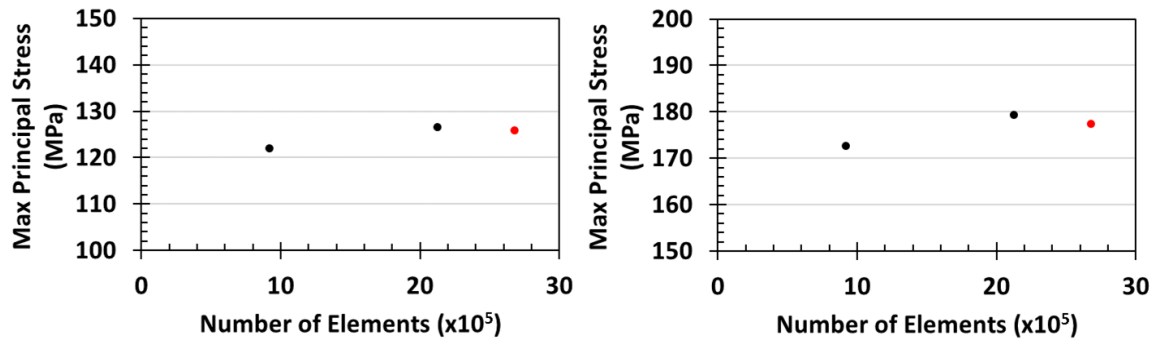


Figure 69. Change in maximum principal stress of the novel bonding model as the number of elements in the mesh was increased, showing the stress in the AlN (Left), and the stress in the bond material (Right). The mesh size used for further modeling was indicated by the red marker.

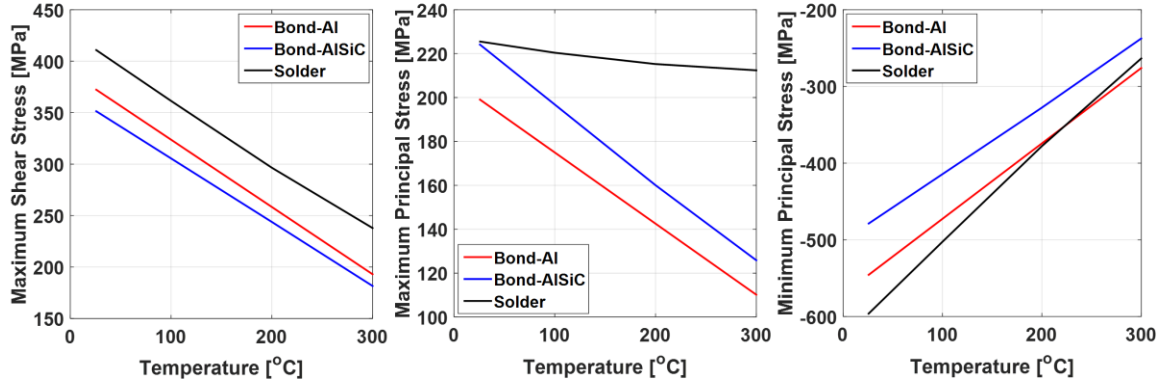


Figure 70. Maximum shear stress (Left), maximum principal stress (Middle), and minimum principal stress (Left) in the AlN body for the DBC with solder joint, the bond modeled with the CTE of Al, and the bond with the CTE of AlSiC.

For the AlN layer, the shear stress of the bonded model was lower than the DBC model for both the CTE of Al and AlSiC. The maximum principal stress for the DBC model was larger than the stress for either the Al or AlSiC models, and this difference increased with temperature. The maximum principal stress is tensile so it is responsible for pulling cracks open, so decreasing this implies cracking will be less likely in the AlN layer using this bond. Finally, the minimum principal stress was also less negative for both models until ~220 °C. This means that for almost all cases, the AlN undergoes less stress than in the solder case, so cracking should be less prevalent in the bonded sample.

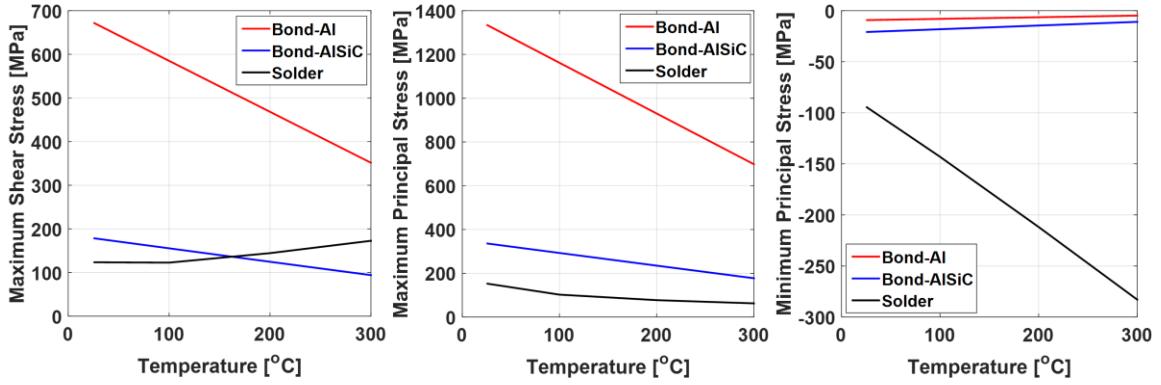


Figure 71. Maximum shear stress (Left), maximum principal stress (Middle), and minimum principal stress (Left) in bond material for the DBC with solder joint, the bond modeled with the CTE of Al, and the bond with the CTE of AlSiC.

For the baseplate attach layer, (being solder in the DBC model, and the new bond for the integrated method), the maximum shear stress was lower for the DBC model until $\sim 180^{\circ}\text{C}$ when the AlSiC dropped below it. However the bond with the CTE of Al was much higher, implying the ratio of SiC in the bond will be a very important parameter to mechanical behavior. The minimum principal stress was significantly lower in both the bonded models than the DBC model, and were nearly zero. For the maximum principal stress the DBC model was lower in all cases, however the bond with the CTE of Al was almost seven times larger than the solder. The hardness of the bond, (measured to be 6.3 GPa) was also higher than the hardness of AuSn solder, (~ 1.7 GPa [109]). Therefore, the bond material also has a greater ability to resist permanent plastic deformation, even for the cases where stresses in the bond were higher. This shows a potentially massive improvement to reduce delamination and cracking in the AlN material compared to solder methods.

3.6 Finite Element Modelling of Thermal Performance

In order to estimate the potential thermal improvement by bonding the AlN layer directly to the AlSiC heat spreader a comparative study was performed in ANSYS. In this study a representative IGBT module was designed, based on the ABB HiPak module with 6 integrated IGBTs [91], similar to the IGBT model used in Chapter 2. In order to reduce computational time of the model the system was reduced to a single unit cell of the HiPak module as shown above in Figure 66. The location of the heat load and convective boundary condition are shown in Figure 72.

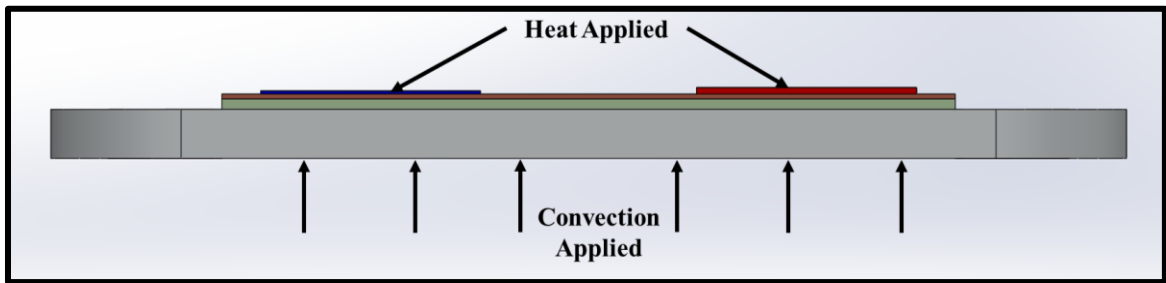


Figure 72. Diagram showing the location of the applied heat load and convective boundary on the bonded baseplate model.

The power substrate was comprised of an AlN layer with a copper metallization layer on top, and a 3 mm AlSiC layer bonded to the bottom. The IGBTs and diodes were given the properties of silicon. The Au-Sn solder between the chips and copper layer and the bond between the AlN and AlSiC were modeled as thermal interface conductances of 0.877, and 0.826 K-m²/MW, respectively. These values were computed from the thermal conductivities and layer thicknesses given in Table 9.

Table 9. Thermal properties and thicknesses of materials used in numerical model.

Material	Thermal Conductivity (W/m-K)	Thickness (μm)
Silicon	130	190 (IGBT), 390 (Diode)
Au-Sn Solder	57	50
Copper	385	300
AlN	157	630
AlSiC	185	3000
AlN/AlSiC bond	121	100

The heat applied the IGBTs and the diodes was split 85.7% to the IGBTs, and 14.2% to the diodes. This power split estimate was based on modeling by Narumachi et al. which was performed on an inverter for a Toyota Prius [28]. Several heat transfer coefficients were applied to the backside of the baseplate in order to simulate the typical values realized by different cooling technologies. The cooling fluid temperature was maintained at 30°C.

Table 10. Model parameters applied the bonded IGBT, indicating the type of cooling solution which would result in similar values of heat transfer coefficient [110].

Heat Transfer Coefficient (W/m ² -K)	Power (W)
500 (forced convection, air)	100
1000 (free convection, liquid)	300
5000 (forced convection, liquid)	500
15,000 (forced convection/evaporation)	700
50,000 (boiling/phase change)	-

Since it was already shown in Chapter 2 that this model does not have a very high dependence on the mesh size, mesh refinement was not performed. A mesh with a similar number of elements to the mesh in Chapter 2 was used for this model as well. The maximum temperature was recorded for each unique combination of heat transfer coefficient and applied power. The maximum temperature on the model, indicated in Figure 73, was plotted as a function of heat load for different heat transfer coefficients below in Figure 74. The maximum temperature was always found on the bottom center

IGBT chip since the bottom center chip always had the least space available around it for heat spreading, as it was surrounded by two diodes.

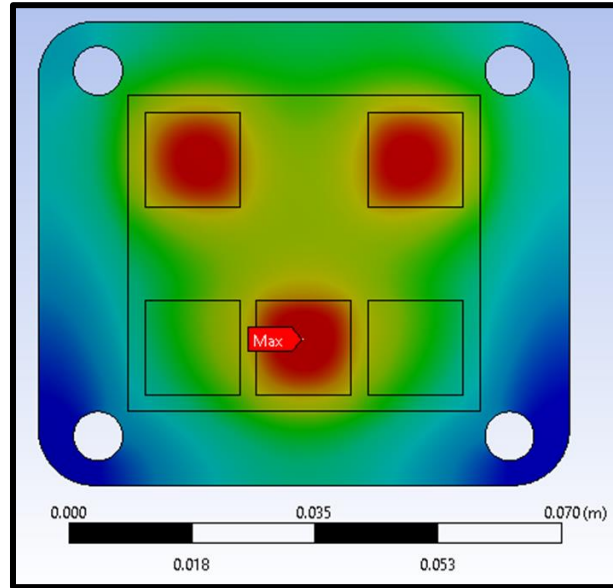


Figure 73. Temperature distribution of the IGBT module showing the location of the maximum temperature on the model with a red flag.

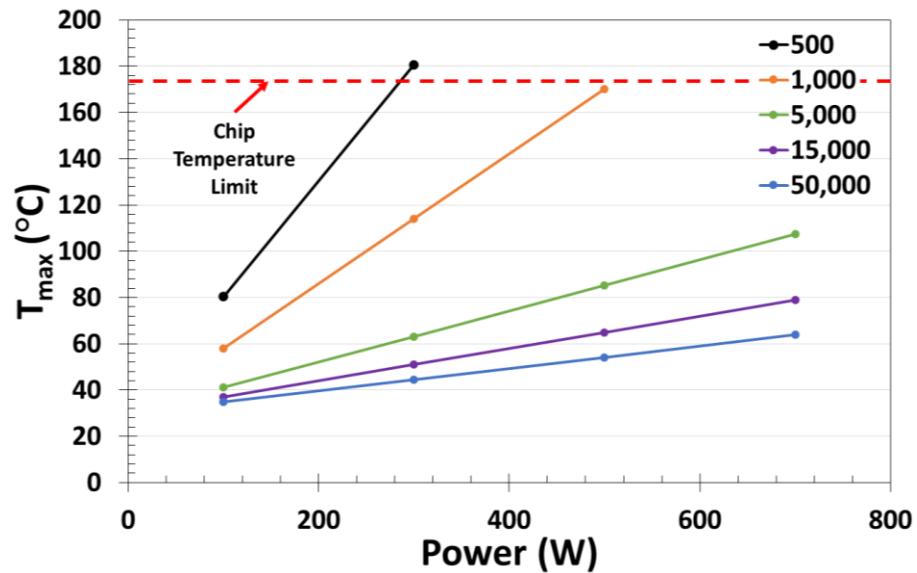


Figure 74. Maximum temperature of the bonded AlSiC model plotted against heat load with several different representative heat transfer coefficients applied to the backside.

The maximum temperatures for the 500 and 1,000 W/m²-K HTC values which significantly overshoot the maximum chip temperature are not shown in Figure 74. The soldered DBC model behaved nearly identically however the maximum temperature averaged 1.65°C lower than the bonded AlSiC model. Since the value for the solder layer was almost identical to the value of the bond layer, the higher temperature in the bond model was most likely due to the removal of the 300 µm copper metallization of the DBC. Since this layer was near the IGBT heat source it spread heat slightly more to reduce the temperature. This modeling approach also shows that a heat transfer coefficient between 1,000, and 5,000 W/m²-K would be sufficient to maintain chip temperatures below the limit. This means that forced convection of liquid could maintain the IGBT in the bonded AlSiC/AlN package. This bonding method could also be applied to other classes of power devices such as RF amplifiers which dissipate less heat, but generate significantly higher heat fluxes. In the future work of next chapter the thermal performance of a new high power GaN RF amplifier package using this bonding technique to attach the heat spreader to the baseplate is investigated.

CHAPTER 4. CONCLUSIONS AND FUTURE WORK

4.1 Summary of Results

The experimental and numerical results presented have investigated the direct integration of cooling and heat spreading into the substrate level of power electronics devices. Two different approaches were made, integrating evaporative cooling on the backside of DBC with sintered copper particles, and bonding an AlN substrate directly to an AlSiC baseplate. The evaporative cooler was characterized by the thermal resistance, heat transfer coefficient, and capillary pumping power for different wick thicknesses and sizes. Modeling with ANSYS was then performed to estimate the heat transfer coefficient required for integrated DBC cooling to be an improvement upon cooling with a baseplate. In order to characterize the novel bonding method between AlN and AlSiC the Young's modulus, hardness, and thermal conductivity of the bond were measured experimentally. These properties were then used to model the thermal behavior of this method over a solder attached baseplate. The bond line was also examined under an SEM microscope with EDS to determine its composition, and track the diffusion of species. Through the combination of experimentation and modeling it was shown that the integration of cooling would only be useful with certain cooling methods with high heat transfer coefficients.

Previous studies with evaporative cooling from copper wicks have employed either spherical particles or a sintered copper mesh, while this one used irregularly shaped particles. It was shown that with these irregularly shaped particles, $\sim 10\text{ }\mu\text{m}$ in size, changing the wick thickness between 0.636 and 1.138 mm had almost no effect on the heat thermal resistance. However, increasing the thickness did serve to increase the applied heat

flux manageable before wick dry out occurred. Analytical modeling showed this was due to the increased available area through which capillary pressure drove fluid to the heated surface. Through analytical modeling the capillary performance of the wick was shown to be significantly improve due to the reduced viscosity of water at higher temperatures. The possible effect of wick porosity was shown to be small for thicker wicks as the amount of fluid flow area is already increased by increasing the thickness. However, for thin wicks the porosity must be larger to accommodate the restricted area. The effect of changing particle size was very small for all wick thickness, as long as the particle size was ~ 10 to $25\text{ }\mu\text{m}$. Studying the width of the integrated wick showed that the width had a minimal effect on the thermal resistance as well. As the significant portion of the heat was lost in the central area, so increasing to larger areas had a negligible impact on performance. Similarly, to wick thickness however, increasing the width did increase the heat flux at which surface dry out began to take place. Increasing the width also had a minimal impact on the capillary pumping power, as most of the fluid was absorbed within the central 20 mm of the wick. By applying the measured evaporative heat transfer coefficient to numerical modeling it was determined that integrated evaporation would not be ideal to cool IGBT power devices over a standard AlSiC baseplate model as at least $35\text{ kW/m}^2\text{-K}$ would be needed . However by boiling from a sintered copper surface and reaching HTC values over $70\text{ kW/m}^2\text{-K}$ the integrated cooling method could reduce temperatures below even that of a copper baseplate. This is an easily attainable possibility as HTC values of up to $280\text{ kW/m}^2\text{-K}$ have been attained with boiling before.

Another method investigated for bringing the cooling solution closer to the device was bonding the AlN dielectric layer directly to an AlSiC baseplate. Past methods have

implemented similar approaches to bonding aluminum or copper directly to AlN, however they must then go on to solder the metal to the baseplate. Using SEM imaging and EDS analysis the bond was shown to be composed of 93.0 wt.% Al, 0.6 wt.% C, 1.5 wt.% Cu, 0.3 wt.% N, 1.7 wt.% O, and 2.8 wt.% Si, meaning the Cu had diffused through the bulk of the AlSiC layer. The aluminum was also seen to migrate into the AlN layer approximately 100 μm , leading to a strong bond between the AlN and the AlSiC. The dielectric blocking strength of the AlN/AlSiC was then measured to be the same as the received AlN, so the processing did not affect the dielectric properties of the AlN. The mechanical strength of the bond was characterized by the Young's modulus and the hardness measured by nanoindentation. The Young's modulus was measured to be 83.7 GPa, with a hardness of 6.3 GPa, which were both higher than pure Al, making the bonds more resistant to deformation. The thermal conductivity of the bond was found to be 121.2 W/m-K, approximately twice that of solder, with an average thickness of 100 μm . Finally several samples were thermally cycled and lasted over 100 cycles between -60°C, and 200°C, which was approximately double the typical lifetime of DBC. Finite element stress modeling was then used with the measured properties to show that this novel bonding method would also decrease the stress in the AlN layer to reduce cracking in the ceramic. The measured thermal conductivity was used in a finite element IGBT model to show that this bonding method had an average maximum temperature only 1.65°C higher than the DBC substrate. Therefore, this bonding method maintains similar thermal performance to DBC while improving the mechanical lifetime, and reducing stresses of the device.

4.2 Future Work

4.2.1 *Continued Evaporation and Bonding Work*

Evaporation directly from the backside of DBC is an effective cooling method, but the presented work was only an initial step towards making this method viable. Further studies must focus on the optimization of design parameters such as the wick dimensions, and particle size/shape depending on the power requirements of the system. The permeability also needs to be further investigated for irregularly shaped particles as this was a significant source of uncertainty for the estimated viscous pressure drop. In order to ensure reliable operation of the evaporator, the DBC/Cu particle interface should be thermally cycled as well to make sure it will not delaminate from the DBC. By performing these studies it would be possible to determine under what conditions a cooling method such as this is a viable option.

The novel AlN/AlSiC bonding approach showed a proof of concept for a method to more reliably attach the baseplate into a power electronics stack. However, several more experiments should be performed to ensure both the accuracy of the presented results, and further investigate other applications. Since the bond thickness varied by up to 100% across even a single sample, the resulting thermal conductivity measurements may not be truly representative of the bond. Thermal conductivity should also be measured before thermal cycling, as well as every set number of cycles. This would give a much better image of when the layer becomes too detached to effectively cool the chip anymore. Lastly the shearing stress required to break the bond should be measured, to better approximate the stresses required to cause delamination. Once the bond has been fully characterized with

AlN/AlSiC similar methods can also be tested using other MMCs such as CuMo, and CuW to bond to AlN. These experiments would allow for a full understanding of the possible gains that could be achieved by using a bonding technique such as this.

Directly integrating a heat spreader into a novel RF amplifier package with glass fan-out was shown by this work to be able to reduce the maximum temperature significantly. However, the feasibility and reliability of this type of integration must also be investigated. Due to the high operational temperatures of WBG GaN devices investigating the effects of thermal cycling on the solder joints would be extremely important. The diamond/CuMo interface would also be of importance to investigate as there is a large CTE mismatch which could cause significant problems at these elevated temperatures. It may be required to investigate several polymer based die attach methods which tend to have good ability to join materials with dissimilar CTEs at the cost of thermal performance. Lastly, to more accurately determine the power output of this device transient modeling should be performed since these devices do not typically operate as always-ON. Further investigation of the reliability of an integrated heat spreader would be able to ensure continuous, high power and high temperature operation while in the field.

4.2.2 Modelling an RF chip with integrated heat spreading

High power RF and mm-wave IC's made with wide band gap (WBG) semiconductors such as GaN and GaAs have recently gained traction in commercial applications such as 5G, IoT networks, and even virtual reality. Although they have long been in use in military applications reliable fabrication of GaN HEMTs has only recently advanced to the point of being commercially viable [111]. Due to the use of WBG

semiconductor materials in RF devices they can operate at high temperatures with higher localized heat fluxes than previous silicon devices [112]. These HEMT amplifiers must also operate efficiently, with ultra-low loss packages to allow for high frequency use. In the past these packages have been made of ceramics or metals, which have problems with miniaturization, and have a high cost from small panel sizes. More recent packages have been developed with wafer level fan-outs which significantly increases the pin count, but due to low temperature epoxy used, the power is limited [113]. This creates a need for new package materials that can meet the high thermal requirements while still allowing for high frequency use. A Glass Fan-Out (GFO) is a promising prospect for new packing material due to the low dielectric losses, however glass has a very low thermal conductivity. By integrating a copper heat spreader into a GFO package the heat can be more effectively removed while maintaining high frequency and power operation.

In order to determine the potential effectiveness of these packages, thermal modeling is important as the device reliability is dependent on the maximum channel operating temperature. To qualify a new package design it is necessary to determine how the heat spreader design will affect the channel temperature during operation. It is also important to determine potential cooling solutions at the system level for high power operation. In this study three chip models were used to evaluate the heat spreader size effects, and to evaluate different convective coefficients on the back of a representative package model. The representative package model was also investigated with the bonding method from Chapter 3 to compare to the standard solder attach method.

4.2.2.1 RF Package Model Description

In order to model the glass fan-out package (GFO) first a representative RF amplifier chip was modeled. The chip model was based on the TriQuint TGA2814 GaN power amplifier which has a maximum channel temperature of 275°C, and a maximum power dissipation of 166 W, [114]. The chip was modeled as 75 μm thick SiC with a 2 μm layer of GaN on top of it using temperature dependent thermal conductivity for both materials and a thermal boundary resistance (TBR) of 33 $\text{m}^2\text{-K/GW}$ at the interface. The thermal properties of all the materials used during modeling are summarized below in Table 11. The heat load was applied to the transistors shown in Figure 75 below in the red. The total heat loads applied were split between the large and small areas with 82.5% applied to the large transistor area, and 17.5% applied to the smaller transistor area. This ratio was determined by the ratio of the transistor length in each area compared to the total length of the transistors. The chip was modeled with half-symmetry along the center line to reduce the computational time required.

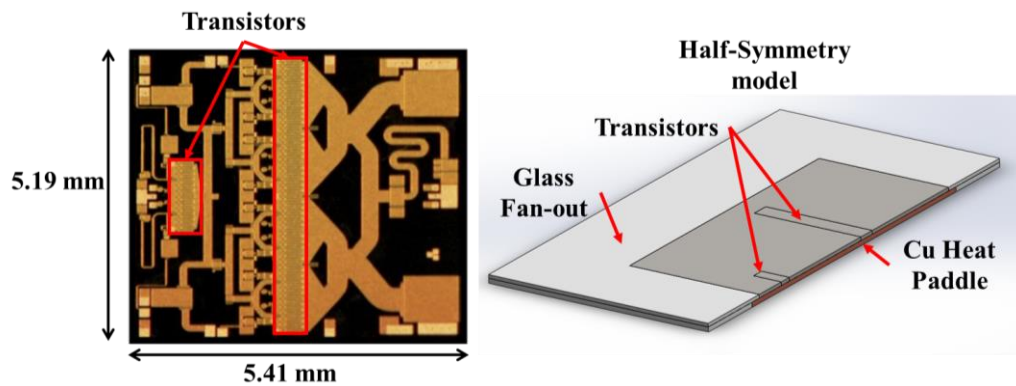


Figure 75. Image of TriQuint TGA2814 GaN power amplifier (Left) and the full package model (Right) showing the location of the two different transistors areas, and the dimensions.

Table 11. Material thermal properties and thicknesses used during modeling.

Material	Thickness	Thermal Conductivity (W/m-K)
GaN, [18]	2 μm	$150 \times \left(\frac{T}{300}\right)^{-1.4}$, 4.1
SiC, [23]	75 μm	$387 \times \left(\frac{T}{293}\right)^{-1.49}$, 4.2
Glass	75 μm around chip, varied around Cu	1.4
Copper	varied	385
Diamond	varied	2000
Aluminum	35 mm	237
CuMo (80/20)	0.5 mm	200
AlSiC	3 mm	185
Au-Sn Solder	50 μm	57
Dow Corning TC-5022	25 μm	4.0

The overall size of the base GFO package was 10 by 10 mm, with a 7 by 7 mm area available to place the chip within. This package was modeled on a heat sink, and attached with Au-Sn solder as shown in Figure 76. The top and sides of the package and heat sink were modeled as adiabatic so all heat was generated in the GaN and dissipated from the bottom of the heat sink. The solder layers were modeled as a TBR of $0.877 \text{ m}^2\text{-K/MW}$, computed from the thickness and thermal conductivity.

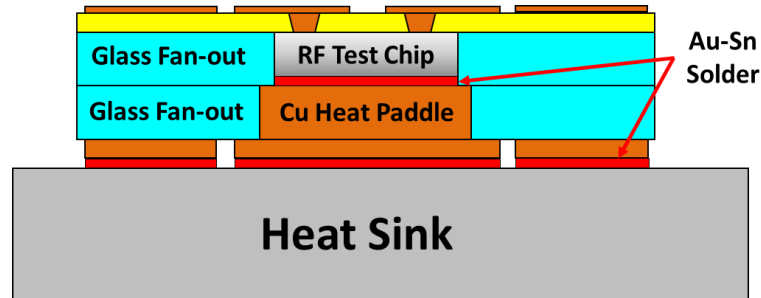


Figure 76. Diagram showing the GFO package with the glass fan-out, copper heat paddle, RF chip, the heat sink, and solder attach locations.

In order to verify that this model results were not dependent on the mesh size, the mesh was refined until the maximum temperature changed by less than 2%. The results of this study are shown in Figure 77 for a 100 μm paddle thickness. A similar number of mesh elements was used for each of the different paddle size models.

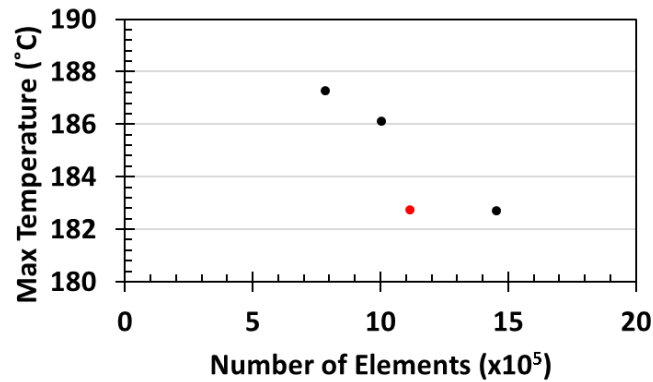


Figure 77. Change in maximum temperature as the number of elements in the mesh was increased, showing the mesh size used for further modeling indicated by the red marker.

4.2.2.2 Heat Paddle Area Study Results

In order to investigate the effect of different heat paddle areas on the maximum temperature of the chip, the package was modeled on an aluminum heat sink, with a constant temperature boundary condition on the bottom. The heat paddle thickness was maintained at 100 μm and the heat sink was 60 by 60 by 35 mm with 30°C set as the constant temperature boundary condition as shown in Figure 78.

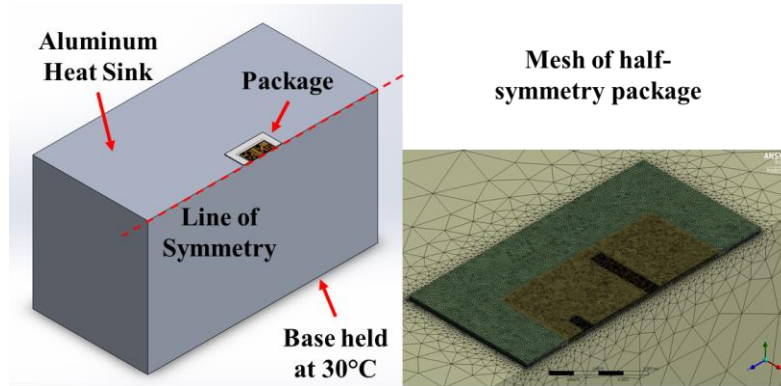


Figure 78. Half symmetry model used evaluated in ANSYS showing the full model on the left with the constant temperature boundary condition, and the package mesh on the right.

The Al heat sink was used so that the performance of the package would be independent of an applied heat transfer coefficient. Heat paddle sizes of 7 by 7 mm, 8.5 by 8.5 mm, and 10 by 10 mm were compared with constant thickness of 100 μm to determine a relationship between the area and the operating temperature of the package. Heat loads of 10, 50, 100, and 150 W were applied to the transistors. The maximum temperature on the package was then recorded for each heat paddle size, and heat load.

Increasing the area of the heat paddle did not significantly reduce the maximum temperature so a representative temperature distribution for the 7 by 7 mm model is shown below in Figure 79. The maximum temperature was always found at the top of the GaN layer at the centre of the large transistor area as was expected.

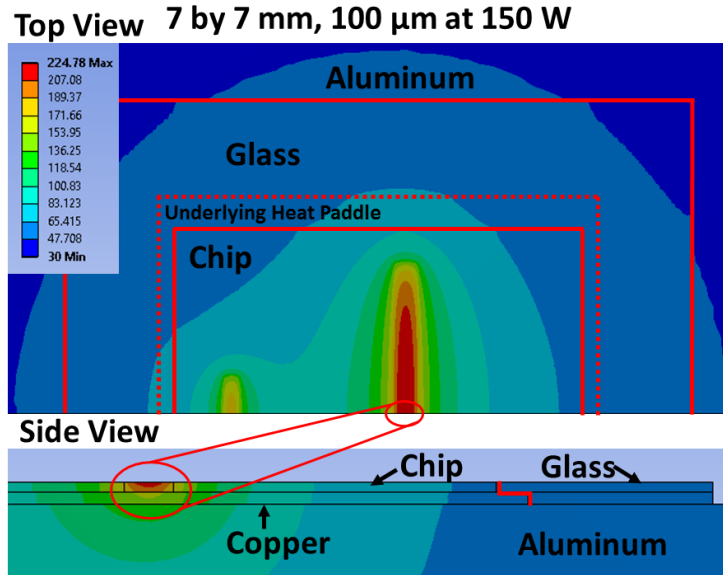


Figure 79. Typical temperature distribution in the package shown for the 7 by 7 mm sample, with a 150 W total heat load applied. The dotted line indicates the area of the underlying heat paddle to show the degree of spreading within the paddle.

Even for the smallest area, 7 by 7 mm, the temperature did not change much around the edges of the Cu heat paddle, implying that lateral heat spreading was minimal at this point. This can be seen in Figure 80, where the maximum temperature recorded does not change significantly as a function of heat paddle area. The largest temperature reduction seen between the 7 by 7 mm and the 10 by 10 mm models occurred at 150 W of applied power, and was only $\sim 3^{\circ}\text{C}$.

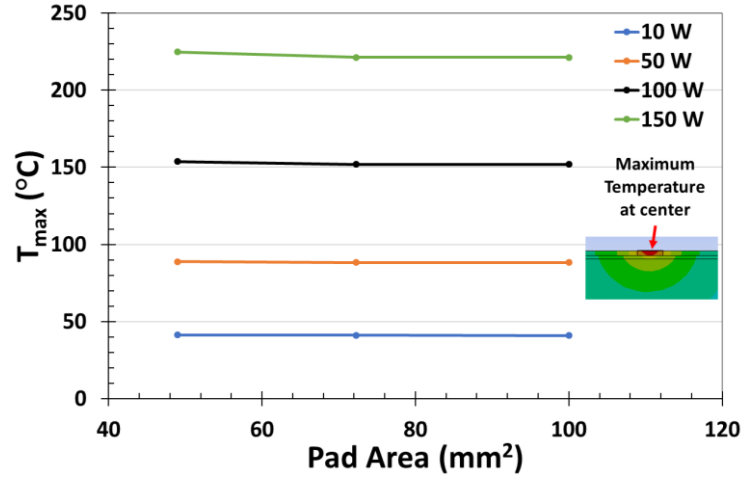


Figure 80. Plot showing the maximum temperature as a function of the heat paddle area for 10, 50, 100, and 150 W. This plot shows how the temperature does not change much as a function of the area.

4.2.2.3 Heat Paddle Thickness Study Results

The previous section showed that the 7 by 7 mm sample was able to adequately spread the heat generated by the GaN transistors, therefore the effect of the thickness of the heat paddle will be investigated in this section. While maintaining the 7 by 7 mm size, heat paddles with thicknesses of 25, 50, 100, 150, and 200 μm were modelled. Similarly to the area study, the thickness study also applied the same aluminium heat sink with 30°C set as the constant temperature boundary condition as shown Figure 78 before. Heat loads of 10, 50, 100, and 150 W were also applied to the transistors. The maximum temperature of the chip was recorded for each simulation, and is plotted below in Figure 81.

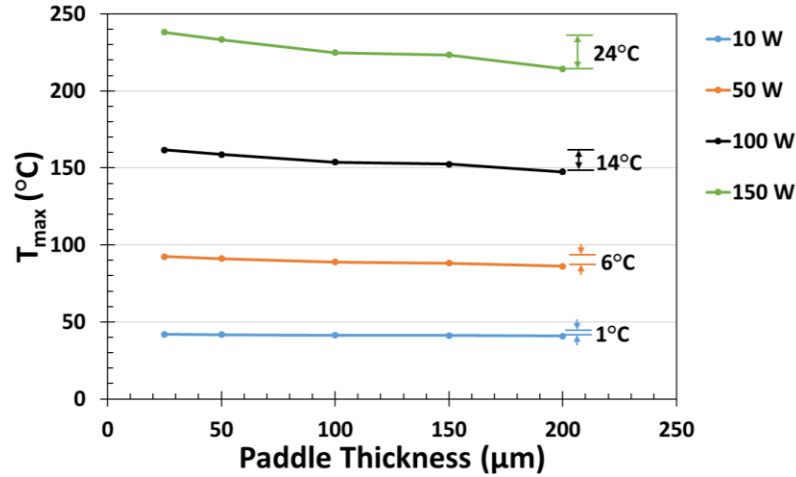


Figure 81. Plot showing the maximum temperature as a function of the heat paddle thickness for 10, 50, 100, and 150 W. The difference between the 25 and 200 μm heat paddles across the heat loads is also indicated by the dimension lines.

This plot shows an improvement of up to 24°C for changing the heat paddle from 25 to 200 μm thick. However the affect was much less pronounced at lower heat loads implying increasing the thickness would only be useful while operating at high heat loads.

Another potential heat spreader for RF devices is chemical vapor deposition (CVD) grown diamond which can have a thermal conductivity between 1000 – 2000 W/m-K at 20°C [115]. The CVD growth process is also able to produce high quality diamond heat spreaders as large 1 mm thick [116]. In order to investigate the largest possible gains from applying a diamond heat spreader, the above models were run again using diamond instead of copper. The thermal conductivity of the copper layer was changed to 2000 W/m-K, while everything else remained the same. The temperature distribution of the package at the edges of the heat spreader in Figure 82 below were comparable to the same location in Figure 79. However, the maximum temperature shown at the center was significantly lower for the diamond heat spreader.

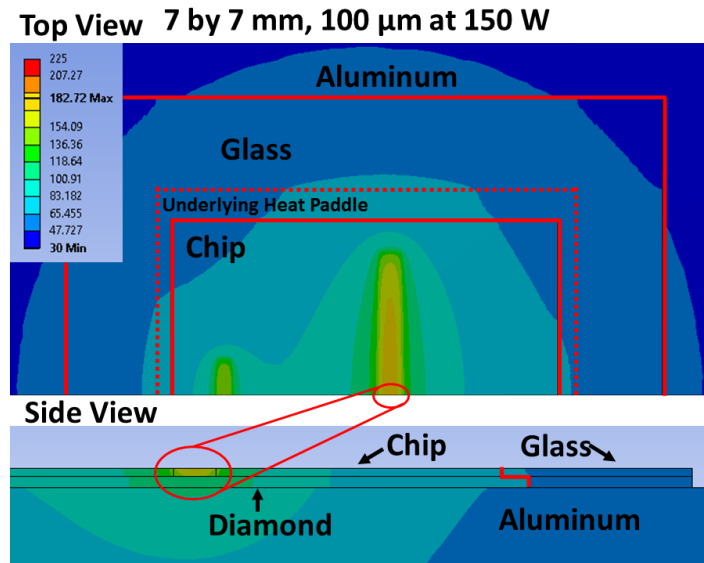


Figure 82. Typical temperature distribution in the package shown for the 100 μ m thick diamond heat paddle, with a 150 W total heat load applied. The dotted line indicates the area of the underlying heat paddle to show the degree of spreading within the paddle.

The difference in maximum temperatures for diamond and copper heat paddles are shown below in Figure 83. At low power levels of ~ 10 W the diamond and copper heat spreaders were comparable, showing less than 5°C difference. However for power levels of 50 W and above the temperature reduction was significant, showing decreases mostly over 10°C . At 150 W the temperature reduction was as much as 47°C implying a potentially dramatic improvement in performance for high power RF devices.

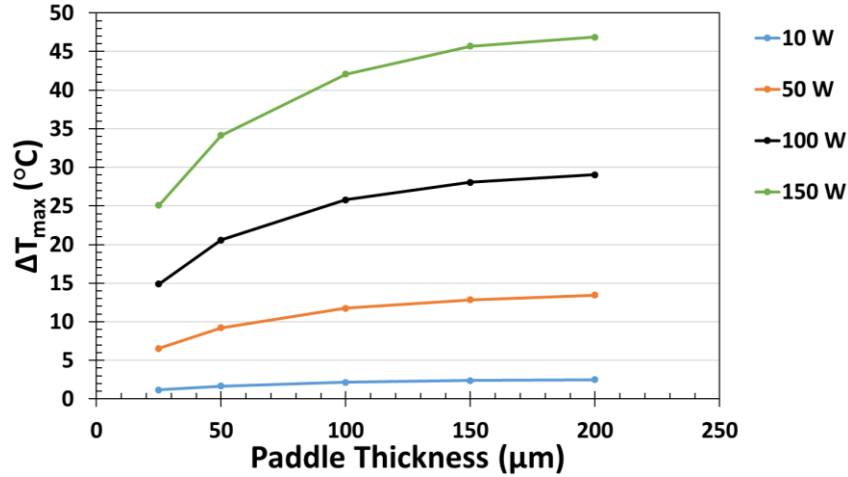


Figure 83. Difference between maximum temperatures of the diamond heat paddle compared to copper for each paddle thickness, showing a maximum of a 47°C decrease in maximum temperature at 150 W by using diamond.

4.2.2.4 Chip Operation with heat sink application

In application this package would be mounted to a thin carrier package, typically a metal matrix composite (MMC), which is then mounted to a copper heat spreader with convective cooling applied to the backside. Therefore in order to determine realistic cooling applications available for this package, another model was used. In the modified model the Cu heat paddle thickness was maintained at 7 by 7 mm area, and thickness of 100 μm. The Al heat sink was replaced with a 20 by 20 by 0.5 mm CuMo (80/20) carrier, which sits atop a 60 by 60 by 3 mm heat spreader as shown in Figure 84. The same TBR of 0.877 m²-K/MW was applied between the package and the CuMo carrier to simulate a solder layer. Another substrate material that is being increasingly used as a heat spreader for high power RF devices is AlSiC, due to the CTE mismatch problems between the CuMo and copper. Therefore the heat spreader was modeled as both solid copper and AlSiC. In typical application the connection between the CuMo carrier and the copper heat spreader

is a thermal grease. For the copper heat spreader model a commercially available thermal grease, (Dow Corning TC-5022), was modeled as a TBR of $6.1 \text{ m}^2\text{-K/MW}$ between the CuMo carrier and the heat spreader. For the AlSiC heat spreader the connection between the CuMo and the AlSiC was modeled as the bond developed in Chapter 3 with a TBR of $0.826 \text{ m}^2\text{-K/MW}$.

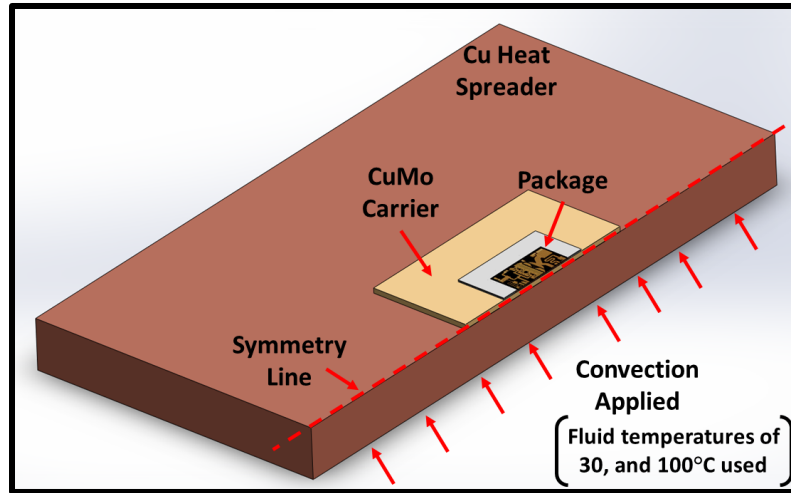


Figure 84. RF package sitting on the CuMo (80/20) carrier, with the heat spreader at the bottom. Showing the location of the applied convection and the ambient fluid temperatures which were used.

In order to verify that this model results were not dependent on the mesh size, the mesh was refined until the maximum temperature changed by less than 2%. The results of this study are shown in figure for a heat transfer coefficient of $5000 \text{ W/m}^2\text{-K}$ with 100 W of power applied.

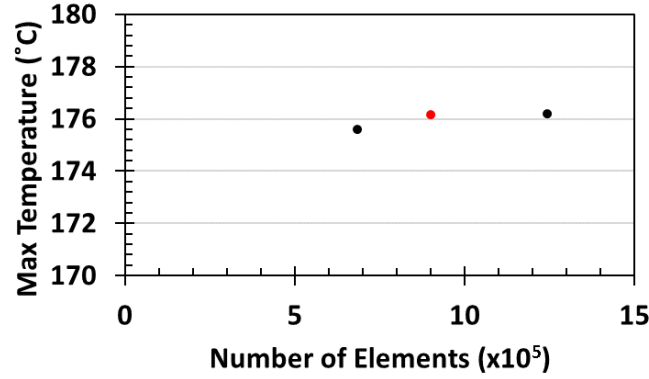


Figure 85. Change in maximum temperature as the number of elements in the mesh was increased, showing the mesh size used for further modeling indicated by the red marker.

Several heat transfer coefficients, and ambient temperatures were applied to the backside at different heat loads and are summarized in Table 12. The heat load applied to the package was split with the same ratio and locations as previously mentioned. The heat transfer coefficients were chosen to be representative of the scale of different convective mechanisms, and not to necessarily represent a specific heat sink design, [110].

Table 12. Model boundary conditions applied to the GFO package on the CuMo (80/20) carrier and copper heat spreader.

Heat Transfer Coefficient ($\text{W}/\text{m}^2\text{-K}$)	Power (W)	Ambient Temperature ($^{\circ}\text{C}$)
500 (forced convection, air)	10	30
1000 (free convection, liquid)	50	100
5000 (forced convection, liquid)	100	-
15,000 (forced convection/evaporation)	150	-
50,000 (boiling/phase change)	-	-
100,000 (boiling/spray cooling)	-	-

The maximum temperature was recorded for each unique combination of heat transfer coefficients, powers, and ambient temperatures. The maximum temperature is shown below for a 30°C , and 100°C fluid temperatures in Figure 86 and Figure 87 respectively for different heat loads, as the heat transfer coefficient is increased. The fluid

temperatures were chosen to represent the likely scenarios where different heat transfer coefficients would be applicable. Although forced convection would be possible with 30°C water, to reach heat transfer coefficients near 50,000 W/m²K phase change would be required. Therefore the system was also modeled at 100°C, the boiling point of water, to represent the likely fluid temperature required to reach larger heat transfer coefficients.

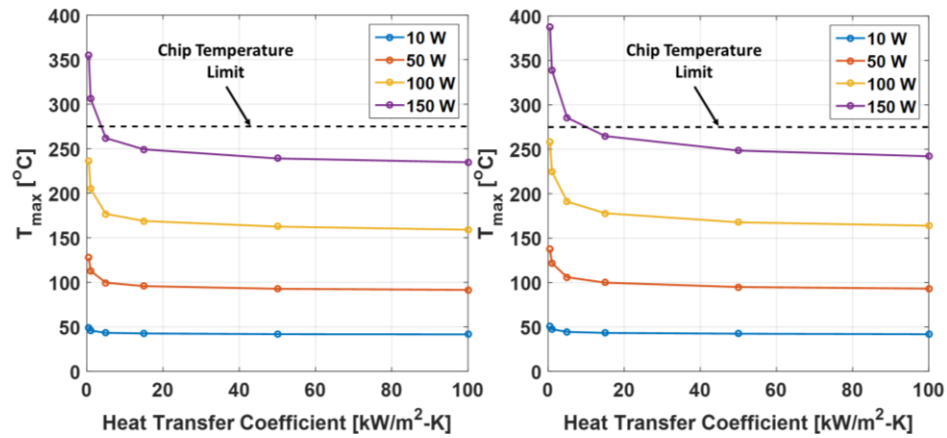


Figure 86. Maximum chip temperature plotted against the heat transfer coefficient for different heat loads, with a 30°C fluid temperature. The plot for the copper heat spreader is shown on the left, while the AlSiC heat spreader is shown on the right.

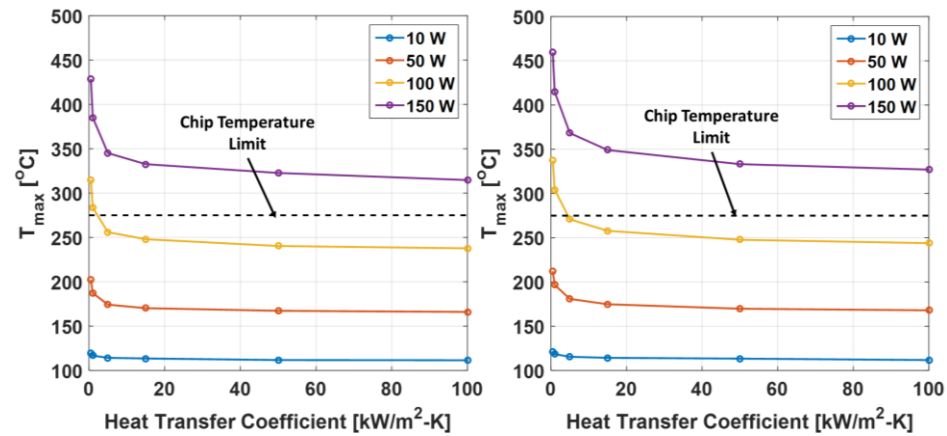


Figure 87. Maximum chip temperature plotted against the heat transfer coefficient for different heat loads, with a 100°C fluid temperature. The plot for the copper heat spreader is shown on the left, while the AlSiC heat spreader is shown on the right.

In all simulations the copper heat spreader had a lower maximum temperature than the AlSiC heat spreader. However the AlSiC spreader was still able to maintain the temperature below the maximum operational chip temperature with similar heat transfer coefficients. In the case of 100°C ambient fluid and 150 W no heat transfer coefficient was able to maintain the temperature below the limit. This means the thermal resistance of the package and heat spreader was the limiting factor to heat transfer. However for the 30°C ambient fluid and 150 W case both the copper and AlSiC heat spreaders were able to reduce the temperature below limiting temperature with a heat transfer coefficient of around 10,000 W/m²-K. This means that boiling would not be a suitable method for cooling this kind of package. However forced convection or evaporation would be able to maintain low temperatures with a sufficiently low fluid temperature.

4.2.2.5 Summary of Modeling

The improved cooling by integrating a heat spreader into a GaN HEMT RF amplifier package with a novel glass-fan-out was investigated through ANSYS modeling. The improvement was characterized by the change in maximum temperature for changes in the spreader size, and material type. The integrated heat spreader package was then modeled on top of a realistic cold plate to estimate the required heat transfer coefficient to operate below the temperature limit. The system was modeled entirely with ANSYS in order to perform parametric studies on the heat spreader size, and material type. The area of the heat spreader had almost no effect on the chip temperature since the heat source was at the center of the chip. With the spreader at a minimum size of the chip temperature, it was already sufficiently large to spreader from the hot spot of the chip. Increasing the thickness

of the paddle from 25 μm to 200 μm was able to reduce the maximum temperature by as much as 24°C at 150 W of applied power. Changing the heat spreader to diamond had an even greater impact, reducing the maximum temperature by an additional 47°C at 200 μm thick. Even with the thinnest heat spreader, 25 μm , the diamond was able to reduce the temperature by as much as 25°C with 150 W of applied heat. Therefore, changing the material would be much more effective than increasing the thickness. The package was then modeled on a representative cold plate with a 100 μm copper heat spreader. It was shown that heat transfer coefficients of about 20 $\text{kW}/\text{m}^2\text{-K}$ would be required to maintain temperatures below the maximum with 30°C fluid temperature. For fluid at 100°C, the current design would not be able to maintain operational temperatures at 150 W of power. However, with a 200 μm thick diamond heat spreader, and an HTC value more than 50 $\text{kW}/\text{m}^2\text{-K}$ the chip could be maintained at operational temperatures with 100°C fluid temperatures. This again demonstrates that diamond heat spreaders may be the most effective method for small scale, in package spreading.

REFERENCES

- [1] F. Blaabjerg, C. Zhe, and S. B. Kjaer, "Power electronics as efficient interface in dispersed power generation systems," *IEEE Transactions on Power Electronics*, vol. 19, pp. 1184-1194, 2004.
- [2] "Wide Bandgap Semiconductors: Pursuing the Promise," U. S. D. o. E. A. M. Office, Ed., ed, 2013.
- [3] T. Kikkawa, K. Joshin, and M. Kanamura, "GaN device for highly efficient power amplifiers," *Fujitsu Sci. Tech. J.*, vol. 48, pp. 40-46, 2012.
- [4] K. Shenai, R. S. Scott, and B. J. Baliga, "Optimum semiconductors for high-power electronics," *IEEE Transactions on Electron Devices*, vol. 36, pp. 1811-1823, 1989.
- [5] B. K. Bose, "Power electronics-an emerging technology," *IEEE Transactions on Industrial Electronics*, vol. 36, pp. 403-412, 1989.
- [6] Z. Chen, J. M. Guerrero, and F. Blaabjerg, "A Review of the State of the Art of Power Electronics for Wind Turbines," *IEEE Transactions on Power Electronics*, vol. 24, pp. 1859-1875, 2009.
- [7] A. Emadi, S. S. Williamson, and A. Khaligh, "Power electronics intensive solutions for advanced electric, hybrid electric, and fuel cell vehicular power systems," *IEEE Transactions on Power Electronics*, vol. 21, pp. 567-577, 2006.
- [8] C. Deline, B. Marion, J. Granata, and S. Gonzalez, "Performance and economic analysis of distributed power electronics in photovoltaic systems," National Renewable Energy Laboratory (NREL), Golden, CO.2011.
- [9] B. Kroposki, "Advanced Power Electronic Functionality for Renewable Energy Integraton with the Power Grid," NREL (National Renewable Energy Laboratory (NREL), Golden, CO (United States))2016.
- [10] Y. F. Wu, J. Gritters, L. Shen, R. P. Smith, J. McKay, R. Barr, *et al.*, "Performance and robustness of first generation 600-V GaN-on-Si power transistors," in *The 1st IEEE Workshop on Wide Bandgap Power Devices and Applications*, 2013, pp. 6-10.
- [11] B. J. Baliga, *The IGBT device: physics, design and applications of the insulated gate bipolar transistor*: William Andrew, 2015.
- [12] A. Satter. Insulated Gate Bipolar Transistor (IGBT) Basics

- [13] K. Sheng, S. J. Finney, and B. W. Williams, "Thermal stability of IGBT high-frequency operation," *IEEE transactions on industrial electronics*, vol. 47, pp. 9-16, 2000.
- [14] P. D. Reigosa, D. Prindle, G. Pâques, S. Geissmann, F. Iannuzzo, A. Kopta, *et al.*, "Comparison of thermal runaway limits under different test conditions based on a 4.5kV IGBT," *Microelectronics Reliability*, vol. 64, pp. 524-529, 2016/09/01/ 2016.
- [15] C. B. C. Bull. 7/11/2016). IGBT or MOSFET: Choose Wisely. 5.
- [16] J. D. Brown, S. Gibb, J. McKenna, M. Poulton, S. Lee, K. Gratzner, *et al.*, "Performance, reliability, and manufacturability of AlGaIn/GaN high electron mobility transistors on silicon carbide substrates," *ECS Transactions*, vol. 3, pp. 161-179, 2006.
- [17] M. D. Kamatagi, N. S. Sankeshwar, and B. G. Mulimani, "Thermal conductivity of GaN," *Diamond and Related Materials*, vol. 16, pp. 98-106, 1// 2007.
- [18] A. Sarua, H. Ji, K. P. Hilton, D. J. Wallis, M. J. Uren, T. Martin, *et al.*, "Thermal Boundary Resistance Between GaN and Substrate in AlGaIn/GaN Electronic Devices," *IEEE Transactions on Electron Devices*, vol. 54, pp. 3152-3158, 2007.
- [19] D. Altman, M. Tyhach, J. McClymonds, S. Kim, S. Graham, J. Cho, *et al.*, "Analysis and characterization of thermal transport in GaN HEMTs on Diamond substrates," in *Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm)*, 2014 IEEE Intersociety Conference on, 2014, pp. 1199-1205.
- [20] H. Shibata, Y. Waseda, H. Ohta, K. Kiyomi, K. Shimoyama, K. Fujito, *et al.*, "High thermal conductivity of gallium nitride (GaN) crystals grown by HVPE process," *Materials Transactions*, vol. 48, pp. 2782-2786, 2007.
- [21] O. Ambacher, B. Foutz, J. Smart, J. Shealy, N. Weimann, K. Chu, *et al.*, "Two dimensional electron gases induced by spontaneous and piezoelectric polarization in undoped and doped AlGaIn/GaN heterostructures," *Journal of applied physics*, vol. 87, pp. 334-344, 2000.
- [22] K. Joshin, T. Kikkawa, S. Masuda, and K. Watanabe, "Outlook for GaN HEMT technology," *Fujitsu Sci. Tech. J*, vol. 50, pp. 138-143, 2014.
- [23] "Thermal conductivity and electrical properties of 6H silicon carbide," *Journal of Applied Physics*, vol. 50, pp. 5790-5794, 1979/09/01 1979.
- [24] F. Miyashiro, N. Iwase, A. Tsuge, F. Ueno, M. Nakahashi, and T. Takahashi, "High thermal conductivity aluminum nitride ceramic substrates and packages," *IEEE Transactions on Components, Hybrids, and Manufacturing Technology*, vol. 13, pp. 313-319, 1990.

- [25] J. H. Harris, "Sintered aluminum nitride ceramics for high-power electronic applications," *JOM*, vol. 50, pp. 56-60, 1998.
- [26] J. King, *Materials Handbook for Hybrid Microelectronics*. Norwood, MA: Artech House, 1988.
- [27] M. A. Occhionero, R. A. Hay, R. W. Adams, and K. P. Fennessy, "Aluminum silicon carbide (AlSiC) for cost-effective thermal management and functional microelectronic packaging design solutions," in *12th European Microelectronics and Packaging Conference*, 1999.
- [28] S. Narumanchi, M. Mihalic, K. Kelly, and G. Eesley, "Thermal interface materials for power electronics applications," in *2008 11th Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems*, 2008, pp. 395-404.
- [29] M. B. Alan Ristow, Aleksander Pregelj, Ajeet Rohatgi, "Development of a Methodology for Improving Photovoltaic Inverter Reliability," *IEEE TRANSACTIONS ON INDUSTRIAL ELECTRONICS*, vol. 55, p. 11, June 6, 2016 2008.
- [30] J. E. R. T. Dustin A. Murdock, Jeffrey J. Connors, Robert D. Lorenz, "Active Thermal Control of Power Electronic Modules," *IEEE TRANSACTIONS ON INDUSTRY APPLICATIONS*, vol. 42, p. 7, June 6, 2016 2006.
- [31] G. Meneghesso, G. Verzellesi, F. Danesin, F. Rampazzo, F. Zanon, A. Tazzoli, *et al.*, "Reliability of GaN high-electron-mobility transistors: State of the art and perspectives," *IEEE Transactions on Device and Materials Reliability*, vol. 8, pp. 332-343, 2008.
- [32] N. Valentine, D. Das, and M. Pecht, "Failure Mechanisms of Insulated Gate Bipolar Transistors (IGBTs)," in *NREL Photovoltaic Reliability Workshot*, Golden Colorado, 2015, p. 30.
- [33] H. Lu, C. Bailey, and C. Yin, "Design for reliability of power electronics modules," *Microelectronics Reliability*, vol. 49, pp. 1250-1255, 2009/09/01/ 2009.
- [34] M. Ciappa, "Selected failure mechanisms of modern power modules," *Microelectronics Reliability*, vol. 42, p. 15, June 5, 2016 2002.
- [35] S. Narumanchi, D. DeVoto, M. Mihalic, and P. Paret, "Performance and Reliability of Interface Materials for Automotive Power Electronics (Presentation)," National Renewable Energy Laboratory (NREL), Golden, CO.2013.
- [36] P. C. Paris and F. Erdogan, "A critical analysis of crack propagation laws," 1963.
- [37] W. B. Nelson, *Accelerated testing: statistical models, test plans, and data analysis* vol. 344: John Wiley & Sons, 2009.

- [38] K. K. Thomas Abraham, and Kevin Bennion, "Advanced Thermal Control Enabling Cost Reduction for Automotive Power Electronics," U. S. D. o. Energy, Ed., ed. Dearborn, Michigan: ANSYS Automotive Conference 2008, p. 25.
- [39] M. Held, P. Jacob, G. Nicoletti, P. Scacco, and M.-H. Poech, "Fast power cycling test of IGBT modules in traction application," in *Power Electronics and Drive Systems, 1997. Proceedings., 1997 International Conference on*, 1997, pp. 425-430.
- [40] J. Schulz-Harder, "DBC substrates as a base for power MCM's," in *Proceedings of 3rd Electronics Packaging Technology Conference (EPTC 2000) (Cat. No.00EX456)*, 2000, pp. 315-320.
- [41] G. Strauch, "Method for manufacturing a power semiconductor device and direct bonded substrate thereof," ed: Google Patents, 2003.
- [42] G. Muralidharan, T. N. Tiegs, and R. W. Johnson, "Composite die-attach materials for high-temperature packaging applications," Oak Ridge National Laboratory (ORNL)2006.
- [43] R. Kisiel and Z. Szczepański, "Die-attachment solutions for SiC power devices," *Microelectronics Reliability*, vol. 49, pp. 627-629, 2009/06/01/ 2009.
- [44] J. Tien and G. Masada, "Confirmation of Creep and Fatigue Damage in Pb/Sn Solder Joints," *Journal of Electronic Packaging*, vol. 114, p. 109, 1992.
- [45] S. Choi, J. Lee, F. Guo, T. Bieler, K. Subramanian, and J. Lucas, "Creep properties of Sn-Ag solder joints containing intermetallic particles," *JOM Journal of the Minerals, Metals and Materials Society*, vol. 53, pp. 22-26, 2001.
- [46] A. Mukherjee, J. Bird, and J. Dorn, "Cones and Vietoris-Begle type theorems," *Transactions of the American Society of Metals*, vol. 62, pp. 155-174, 1969.
- [47] J. P. Schaffer, A. Saxena, S. D. Antolovich, T. H. Sanders, and S. B. Warner, *The science and design of engineering materials*: Irwin Chicago, 1995.
- [48] C. Göbl and J. Faltenbacher, "Low temperature sinter technology die attachment for power electronic applications," in *Integrated Power Electronics Systems (CIPS), 2010 6th International Conference on*, 2010, pp. 1-5.
- [49] R. L. Dietz, M. Featherby, and P. K. Margetts, "Silver-filled glass," ed: Google Patents, 1983.
- [50] I. Y. Chien and M. Nguyen, "Low stress polymer die attach adhesive for plastic packages," in *Electronic Components and Technology Conference, 1994. Proceedings., 44th*, 1994, pp. 580-584.

- [51] H. S. Chin, K. Y. Cheong, and A. B. Ismail, "A review on die attach materials for SiC-based high-temperature power devices," *Metallurgical and Materials Transactions B*, vol. 41, pp. 824-832, 2010.
- [52] J. G. Bai, Z. Z. Zhang, J. N. Calata, and G.-Q. Lu, "Low-temperature sintered nanoscale silver as a novel semiconductor device-metallized substrate interconnect material," *IEEE Transactions on components and packaging technologies*, vol. 29, pp. 589-593, 2006.
- [53] T. Wang, X. Chen, G.-Q. Lu, and G.-Y. Lei, "Low-temperature sintering with nano-silver paste in die-attached interconnection," *journal of electronic materials*, vol. 36, pp. 1333-1340, 2007.
- [54] M. Yovanovich and E. Marotta, "Thermal spreading and contact resistances," *Heat Transfer Handbook*, vol. 1, pp. 261-394, 2003.
- [55] R. Prasher, "Thermal interface materials: historical perspective, status, and future directions," *Proceedings of the IEEE*, vol. 94, pp. 1571-1586, 2006.
- [56] F. Sarvar, D. C. Whalley, and P. P. Conway, "Thermal interface materials-A review of the state of the art," in *Electronics Systemintegration Technology Conference, 2006. 1st*, 2006, pp. 1292-1302.
- [57] C. G. Macris, T. R. Sanderson, R. G. Ebel, C. B. Leyerle, and E. Solutions, "Performance, reliability, and approaches using a low melt alloy as a thermal interface material," in *Proceedings IMAPS*, 2004.
- [58] S. S. Kang, "Advanced Cooling for Power Electronics," presented at the Conference on Integrated Power Electronics Systems, Nuremberg, Germany, March, 2012.
- [59] I. Mudawar, "Assessment of high-heat-flux thermal management schemes," *IEEE Transactions on Components and Packaging Technologies*, vol. 24, pp. 122-141, 2001.
- [60] S.-S. Hsieh, R.-Y. Lee, J.-C. Shyu, and S.-W. Chen, "Thermal performance of flat vapor chamber heat spreader," *Energy Conversion and Management*, vol. 49, pp. 1774-1784, 2008/06/01/ 2008.
- [61] J. Schulz-Harder, "Review on highly integrated solutions for power electronic devices," in *Integrated Power Systems (CIPS), 2008 5th International Conference on*, 2008, pp. 1-7.
- [62] A. Abdoli, G. Jimenez, and G. S. Dulikravich, "Thermo-fluid analysis of micro pin-fin array cooling configurations for high heat fluxes with a hot spot," *International Journal of Thermal Sciences*, vol. 90, p. 8, 2015.

- [63] K. Olesen, R. Bredtmann, and R. Eisele, "Shower power: new cooling concept for automotive applications," in *Proceedings of the Automotive Power Electronics Conference, Paris, France, June, 2006*, pp. 21-22.
- [64] M. Shiraishi, K. Kikuchi, and T. Yamanishi, "Investigation of heat transfer characteristics of a two-phase closed thermosyphon," *Journal of Heat Recovery Systems*, vol. 1, pp. 287-297, 1981/01/01/ 1981.
- [65] Z. G. Xu, Z. G. Qu, C. Y. Zhao, and W. Q. Tao, "Pool boiling heat transfer on open-celled metallic foam sintered surface under saturation condition," *International Journal of Heat and Mass Transfer*, vol. 54, pp. 3856-3867, 2011/08/01/ 2011.
- [66] F. Agostini, W. Puckett, R. Nelson, D. Torresin, B. Agostini, and M. Habert, "Experimental Investigation of Enhanced Two-Phase Evaporator Using Aluminum Foams," in *ASME 2015 13th International Conference on Nanochannels, Microchannels, and Minichannels collocated with the ASME 2015 International Technical Conference and Exhibition on Packaging and Integration of Electronic and Photonic Microsystems*, 2015, pp. V001T02A002-V001T02A002.
- [67] S. You, J. Kim, and K. Kim, "Effect of nanoparticles on critical heat flux of water in pool boiling heat transfer," *Applied Physics Letters*, vol. 83, pp. 3374-3376, 2003.
- [68] M. Ha and S. Graham, "Pool Boiling Enhancement through Hierarchical Texturing of Surfaces," presented at the 15th IEEE ITherm Las Vegas, 2016.
- [69] A. F. Ali and M. S. El-Genk, "Spreaders for immersion nucleate boiling cooling of a computer chip with a central hot spot," *Energy Conversion and Management*, vol. 53, p. 9, 2012.
- [70] F. J. Hong, P. Cheng, H. Y. Wu, and Z. Sun, "Evaporation/boiling heat transfer on capillary feed copper particle sintered porous wick at reduced pressure," *International Journal of Heat and Mass Transfer*, vol. 63, p. 11, 2013.
- [71] K. C. Leong, C. Y. Liu, and G. C. Lu, "Characterization of Sintered Copper Wicks Used in Heat Pipes," *Journal of Porous Materials*, vol. 4, p. 6, 1997.
- [72] S. Kalpakjian and S. R. Schmid, *Manufacturing Processes for Engineering Materials*, 5th ed. Upper Saddle River, NJ: Pearson Education, Inc., 2008.
- [73] S. W. Chi, *Heat pipe theory and practice*. Washington, DC: Hemisphere Publishing Corporation, 1976.
- [74] P. C. Carman, "Fluid flow through granular beds," *Chemical Engineering Research and Design*, vol. 75, p. 17, 1997.

- [75] S. V. G. Justin A. Weibel, Mark T. North, "Characterization of evaporation and boiling from sintered powder wicks fed by capillary action," *International Journal of Heat and Mass Transfer*, p. 11, 4/7/2016 2010.
- [76] D. K. Plaks. (2017). *Intrachip/Interchip Enhanced Cooling (ICECool)*. Available: <https://www.darpa.mil/program/intrachip-interchip-enhanced-cooling>
- [77] A. Bar-Cohen¹, J. J. Maurer, and J. G. Felbinger, "DARPA's intra/interchip enhanced cooling (ICECool) program," in *CS MANTECH Conference, May 13th-16th*, 2013.
- [78] G. F. Goth, A. Arvelo, J. Eagle, M. J. Ellsworth, K. C. Marston, A. K. Sinha, *et al.*, "Thermal and mechanical analysis and design of the IBM Power 775 water cooled supercomputing central electronics complex," in *13th InterSociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems*, 2012, pp. 700-709.
- [79] C. T. Creamer, K. K. Chu, P. C. Chao, B. Schmanski, T. Yurovchak, S. Sweetland, *et al.*, "S2-T6: Microchannel cooled, high power GaN-on-Diamond MMIC," in *2014 Lester Eastman Conference on High Performance Devices (LEC)*, 2014, pp. 1-5.
- [80] A. Bar-Cohen, J. J. Maurer, and A. Sivananthan, "Near-Junction Microfluidic Cooling for Wide Bandgap Devices," *MRS Advances*, vol. 1, pp. 181-195, 2016.
- [81] V. Gambin, B. Poust, D. Ferizovic, M. Watanabe, G. Mandrusiak, D. Lin, *et al.*, "Impingement cooled embedded diamond multiphysics co-design," in *2016 15th IEEE Intersociety Conference on Thermal and Thermomechanical Phenomena in Electronic Systems (ITherm)*, 2016, pp. 1518-1529.
- [82] S. Bell, *A beginner's guide to uncertainty of measurement*: National Physical Laboratory Teddington, Middlesex, 2001.
- [83] T. Beechem, S. Graham, S. P. Kearney, L. M. Phinney, and J. R. Serrano, "Simultaneous mapping of temperature and stress in microdevices using micro-Raman spectroscopy," *Review of Scientific Instruments*, vol. 78, 2007.
- [84] A.-J. N. Khalifa, "Natural convection heat transfer coefficient - A review I. Isolated vertical and horizontal surfaces," *Energy Conversion and Management*, vol. 42, p. 14, 2001.
- [85] M. Ivanova, Y. Avenas, C. Schaeffer, J. B. Dezord, and J. Schulz-Harder, "Heat Pipe Integrated in Direct Bonded Copper (DBC) Technology for Cooling of Power Electronics Packaging," *IEEE Transactions on Power Electronics*, vol. 21, pp. 1541-1547, 2006.

- [86] S.-C. Wong, "The evaporation mechanism in the wick of copper heat pipes," in *The Evaporation Mechanism in the Wick of Copper Heat Pipes*, ed: Springer, 2014, pp. 1-36.
- [87] A. Faghri, *Heat Pipe Science and Technology*. Washington, DC: Taylor & Francis, 1995.
- [88] X. Garcia, L. T. Akanji, M. J. Blunt, S. K. Matthai, and J. P. Latham, "Numerical study of the effects of particle shape and polydispersity on permeability," *Physical Review E*, vol. 80, p. 021304, 08/26/ 2009.
- [89] C. Li, G. Peterson, and Y. Wang, "Experimental study of thickness effects on evaporation/boiling on thin sintered copper mesh surfaces," in *ASME 2005 Summer Heat Transfer Conference collocated with the ASME 2005 Pacific Rim Technical Conference and Exhibition on Integration and Packaging of MEMS, NEMS, and Electronic Systems*, 2005, pp. 281-290.
- [90] B. Marcus, "On the operation of heat pipes," *TRW Rep*, pp. 9895-6001, 1965.
- [91] S. H. V. S. D. G. D. E. H. R. S. D. T. C. Papadopoulos, "Packaging Technology Platform for Next Generation High Power IGBT Modules," presented at the PCIM Europe, Nuremberg, 2014.
- [92] "Carbon Nanotube Coatings for Enhanced Capillary-Fed Boiling from Porous Microstructures," *Nanoscale and Microscale Thermophysical Engineering*, vol. 16, pp. 1-17, 2012/01/01 2012.
- [93] H. Bostanci, D. Van Ee, B. A. Saarloos, D. P. Rini, and L. C. Chow, "Spray cooling of power electronics using high temperature coolant and enhanced surface," in *Vehicle Power and Propulsion Conference, 2009. VPPC'09. IEEE*, 2009, pp. 609-613.
- [94] W. MacDonald and T. Eagar, "Transient liquid phase bonding," *Annual review of materials science*, vol. 22, pp. 23-46, 1992.
- [95] Y. N. Yoshirou Kuromitsu, Hiroshi Tonomuru, Kazuhiro Akiyama, Christine Marie Montesa, Naoya Shibata, Yuichi Ikuhara, "Direct bonded aluminum on aluminum nitride substrates via a transient liquid phase and its applications," presented at the International Conference on Integrated Power Electronics Systems, Nuremberg/Germany, 2010.
- [96] W. F. Gale and T. C. Totemeier, *Smithells metals reference book*: Butterworth-Heinemann, 2003.
- [97] C. Deitch, A. Crawford, A. Meier, and R. Fagan, "Surface Preparation of Aluminum Nitride for Metallization: Effect of Temperature on Surface Reactivity," *Materials and Manufacturing Processes*, vol. 20, pp. 863-886, 2005/09/01 2005.

- [98] M. Medraj, Y. Baik, W. T. Thompson, and R. A. L. Drew, "Understanding AlN sintering through computational thermodynamics combined with experimental investigation," *Journal of Materials Processing Technology*, vol. 161, pp. 415-422, 4/30/ 2005.
- [99] (2013). *Aluminum Nitride Engineering Properties*. Available: <http://accuratus.com/alumni.html>
- [100] J. Zhang, Y. N. Huang, C. Mao, and P. Peng, "Structural, elastic and electronic properties of θ (Al₂Cu) and S (Al₂CuMg) strengthening precipitates in Al–Cu–Mg series alloys: First-principles calculations," *Solid State Communications*, vol. 152, pp. 2100-2104, 12// 2012.
- [101] W. Parker, R. Jenkins, C. Butler, and G. Abbott, "Flash method of determining thermal diffusivity, heat capacity, and thermal conductivity," *Journal of applied physics*, vol. 32, pp. 1679-1684, 1961.
- [102] H. J. Lee, "THERMAL DIFFUSIVITY IN LAYERED AND DISPERSED COMPOSITES," 1975.
- [103] R. D. Cowan, "Pulse method of measuring thermal diffusivity at high temperatures," *Journal of Applied Physics*, vol. 34, pp. 926-927, 1963.
- [104] S. Aksöz, Y. Ocak, N. Maraşlı, E. Çadirli, H. Kaya, and U. Büyük, "Dependency of the thermal and electrical conductivity on the temperature and composition of Cu in the Al based Al–Cu alloys," *Experimental Thermal and Fluid Science*, vol. 34, pp. 1507-1516, 2010.
- [105] L. F. Coffin Jr, "A study of the effects of cyclic thermal stresses on a ductile metal," *trans. ASME*, vol. 76, pp. 931-950, 1954.
- [106] G. Mitic, R. Beinert, P. Klofac, H. J. Schultz, and G. Lefranc, "Reliability of AlN substrates and their solder joints in IGBT power modules," *Microelectronics Reliability*, vol. 39, pp. 1159-1164, 1999/06/01/ 1999.
- [107] G. Dong, G. Lei, X. Chen, K. Ngo, and G.-Q. Lu, "Edge tail length effect on reliability of DBC substrates under thermal cycling," *Soldering & Surface Mount Technology*, vol. 21, pp. 10-15, 2009.
- [108] P. Gaiser, M. Klingler, and J. Wilde, "Novel concepts for modelling and enhancing the DBC-Al²-O³ lifetime," in *2016 6th Electronic System-Integration Technology Conference (ESTC)*, 2016, pp. 1-5.
- [109] Y. C. Liu, J. W. R. Teo, S. K. Tung, and K. H. Lam, "High-temperature creep and hardness of eutectic 80Au/20Sn solder," *Journal of Alloys and Compounds*, vol. 448, pp. 340-343, 2008/01/10/ 2008.

- [110] T. L. Bergman and F. P. Incropera, *Introduction to heat transfer*: John Wiley & Sons, 2011.
- [111] J. W. Milligan, S. Sheppard, W. Pribble, Y. F. Wu, G. Muller, and J. W. Palmour, "SiC and GaN Wide Bandgap Device Technology Overview," in *2007 IEEE Radar Conference*, 2007, pp. 960-964.
- [112] J. Millán, P. Godignon, X. Perpiñà, A. Pérez-Tomás, and J. Rebollo, "A Survey of Wide Bandgap Power Semiconductor Devices," *IEEE Transactions on Power Electronics*, vol. 29, pp. 2155-2163, 2014.
- [113] C. C. Liu, S. M. Chen, F. W. Kuo, H. N. Chen, E. H. Yeh, C. C. Hsieh, *et al.*, "High-performance integrated fan-out wafer level packaging (InFO-WLP): Technology and system integration," in *2012 International Electron Devices Meeting*, 2012, pp. 14.1.1-14.1.4.
- [114] "TriQuint TGA2814 " in *3.1-3.6 GHz Power Amplifier*, ed: TriQuint, 2013, p. 13.
- [115] E. Wörner, C. Wild, W. Müller-Sebert, R. Locher, and P. Koidl, "Thermal conductivity of CVD diamond films: high-precision, temperature-resolved measurements," *Diamond and related materials*, vol. 5, pp. 688-692, 1996.
- [116] P. W. May, "Diamond thin films: a 21st-century material," *Philosophical Transactions of the Royal Society of London A: Mathematical, Physical and Engineering Sciences*, vol. 358, pp. 473-495, 2000.